Versatile surrogate models for IC buffers

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Outline

- Introduction
- New approach: theoretical framework
- Identification
- Recent developments
- Examples
- Conclusion





- Assessing
 EMC compatibility
 Signal Integrity
 Reducing
 Design Cost
 Simulation time
 - Time to market









 Nonlinear behavior of IC buffers Fading memory ♦ Highly nonlinear **Switching feature** ♦Saturation Behavioral modeling techniques **♦ IBIS** Mπlog ♦ Neural networks, etc...









- 2-piece model (Mπlog)
 - Black box modeling of buffers
 - Output buffer port modeled in respect to input state (ON or OFF)
 - Transitions between states modeled through weighting functions
 - Output port relations, two submodels scheme









 $\circ \quad \mathsf{I}_2 = \mathsf{f}(\mathsf{v}_2,[\mathsf{k}])$

- Transitions between states modeled through weighting functions
- \circ Dynamic effect of v₁ not in the submodels









- SPI 2010 each submodel represented by SISO Volterra Series
- SPI 2011 mathematical constraints on Volterra series, exact static behavior















I/O behavioral modeling method is :

♦ Versatile

♦wide range of loads

\$ working for a wide range of frequencies

♦ Surrogate

Mathematical models

Based on very high order Volterra-Laguerre Series







- I/O Relations, "admittance", $i_2[k] = f(v_2, v_1, [k])$, "impedance" $v_2[k] = f(i_2, v_1, [k]) =>$
- Behavioral models: high order Volterra-Laguerre series

$$Z\left\{\phi_{n_{l},i_{l}}[k]\right\}(z) = \sqrt{1 - a_{n_{l}}^{2}} \frac{z}{z - a_{n_{l}}} \left(\frac{1 - a_{n_{l}}z}{z - a_{n_{l}}}\right)^{i_{l}}$$

$$\overline{v}_{n_{l},i_{l}}[k] = \left(v_{n_{l}} * \phi_{n_{l},i_{l}}\right)[k], \qquad n_{l} = 1,2$$







$$\begin{split} i_{2}[k] &= \sum_{i_{1}=0}^{I_{1}-1} C_{1,1,i_{1}} \overline{v}_{1,i_{1}}[k] + \sum_{i_{1}=0}^{I_{1}-1} C_{1,2,i_{1}} \overline{v}_{2,i_{1}}[k] \\ &+ \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,1,1,i_{1},i_{2}} \overline{v}_{1,i_{1}}[k] \overline{v}_{1,i_{1}}[k] + \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,1,2,i_{1},i_{2}} \overline{v}_{1,i_{1}}[k] \overline{v}_{2,i_{1}}[k] \\ &+ \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,2,1,i_{1},i_{2}} \overline{v}_{2,i_{1}}[k] \overline{v}_{1,i_{1}}[k] + \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,2,2,i_{1},i_{2}} \overline{v}_{2,i_{1}}[k] \overline{v}_{2,i_{1}}[k] \\ &+ \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,2,1,i_{1},i_{2}} \overline{v}_{2,i_{1}}[k] \overline{v}_{1,i_{1}}[k] + \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,2,2,i_{1},i_{2}} \overline{v}_{2,i_{1}}[k] \overline{v}_{2,i_{1}}[k] \\ &+ \dots \end{split}$$





- Apply a well-chosen identification sequence to the driver.
- Extract voltages (v_1 , v_2) and output current (i_2)
- By least squares find C_m coefficients that satisfied best the Volterra-Laguerre relation

$$i_{2}[k] = \sum_{m=1}^{M} \sum_{n_{1}=1}^{2} \dots \sum_{n_{m}=1}^{2} \sum_{i_{1}=0}^{I_{m}-1} \sum_{i_{m}=0}^{I_{m}-1} C_{m,n_{1},\dots,n_{m},i_{1},\dots,i_{m}} \prod_{l=1}^{m} \overline{v}_{n_{l}}, i_{l}[k]$$









 Variable identification load
 Allowing a good static exploration
 Dynamic exploration of (i₂,v₂) trajectories resulting from interconnects reactive elements





$$\begin{bmatrix} \overline{\varphi}_{1,1,0} \begin{bmatrix} k_0 \end{bmatrix} & \overline{\varphi}_{1,1,1} \begin{bmatrix} k_0 \end{bmatrix} & \dots & \overline{\varphi}_{m\dots} \begin{bmatrix} k_0 \end{bmatrix} \begin{bmatrix} c_{1,1,0} \\ c_{1,1,0} \end{bmatrix} = \begin{bmatrix} i_2 \begin{bmatrix} k_0 \end{bmatrix} \\ i_2 \begin{bmatrix} k_1 \end{bmatrix} \\ \dots \\ \vdots \end{bmatrix} \begin{bmatrix} \overline{\varphi}_{1,1,0} \begin{bmatrix} k_1 \end{bmatrix} & \overline{\varphi}_{1,1,1} \begin{bmatrix} k_1 \end{bmatrix} \\ \dots \\ \overline{\varphi}_{1,1,0} \begin{bmatrix} k_I \end{bmatrix} & \overline{\varphi}_{1,1,1} \begin{bmatrix} k_I \end{bmatrix} \\ \dots \\ \overline{\varphi}_{m\dots} \begin{bmatrix} k_I \end{bmatrix} \end{bmatrix} \begin{bmatrix} k_I \end{bmatrix} \begin{bmatrix} c_{1,1,0} \\ c_{1,1,1} \\ \dots \\ \vdots \end{bmatrix} = \begin{bmatrix} i_2 \begin{bmatrix} k_0 \end{bmatrix} \\ i_2 \begin{bmatrix} k_1 \end{bmatrix} \\ \dots \\ i_2 \begin{bmatrix} k_1 \end{bmatrix} \end{bmatrix}$$





Recent developments

- Piece-wise approach, reduce computational cost, increase precision
- MISO submodels sharing the same internal state
- $\circ \quad \text{Submodel working area defined by } v_1v_2 \ i_2...$







Recent developments



 $i_2[k] = \sum_{i=1}^{I} W_i(v_1) i_{2,i}[k]$ i=1



 Test vehicle: tunable synthetic system mimicking single ended non inverting driver



- \circ f(v₁,v) nonlinear current source
- Dynamic by reactive components







Input/Output static characteristic, different loads





- System is identified through the described procedure
- Volterra Laguerre model is build up
 - 14th order
 - ♦ Total of 190 coefficients
- Implementation in spice simulator
 - Continuous representation
 - Ensuring compatibility, basic elements

Passive components, voltage controlled current sources







Validation Input validation signal On two load configurations









Input validation signal





○ First load, ~2sec,





Second load, non classic, ~2sec





o Cascaded drivers









- System is identified through the described procedure
- Volterra Laguerre model is build up
 - 3 submodels
 - ♦ 5th order submodel
 - ♦ Total of 325 coefficients for each submodel







First Load, ~6sec,





Second load, ~6sec





Conclusion

- A new approach to IC buffer modeling seeking more general, versatile models
 - Based on MISO Volterra-Laguerre Series
 - Can easily take account of another input ex. V_{dd} supply voltage
- Optimization of spice structure, faster simulation
- Ongoing research on more complex, recent buffers
- Tuning the method on the needs of the industry



