



# **Multi-Standard Transceiver for NRZ Serial Communication up to 14Gbps**

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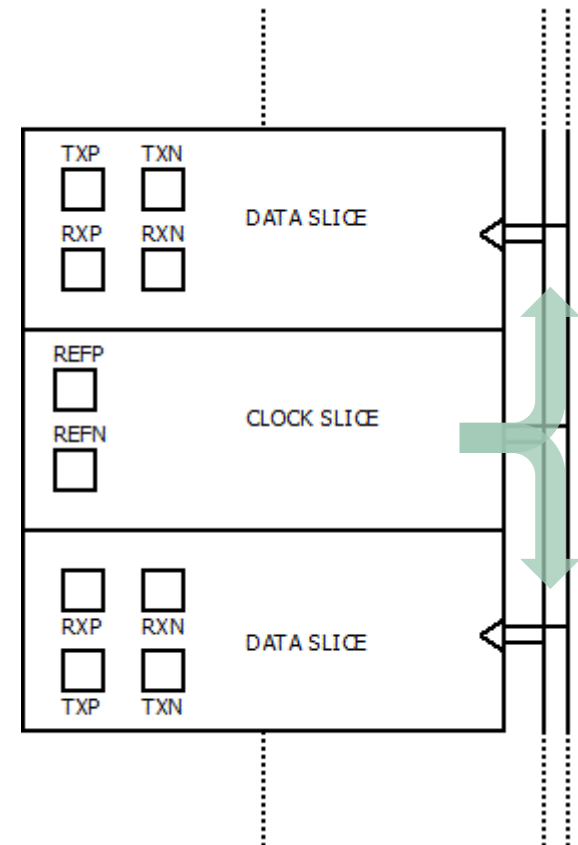
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**May, 2012**

# Multi-Standard Transceiver Highlights



- 32nm CMOSLP technology.
- Single 1V analog supply.
- 0.45mm x 1.3mm SerDes form factor.
- 1.25 to 14.025Gbit/s data rate.
- 220mW power consumption at 14.025Gbit/s.
- More than 22dB channel losses at Nyquist frequency.
- Adaptive 4 taps half rate DFE .
- Programmable 7 taps transmitter FIR.

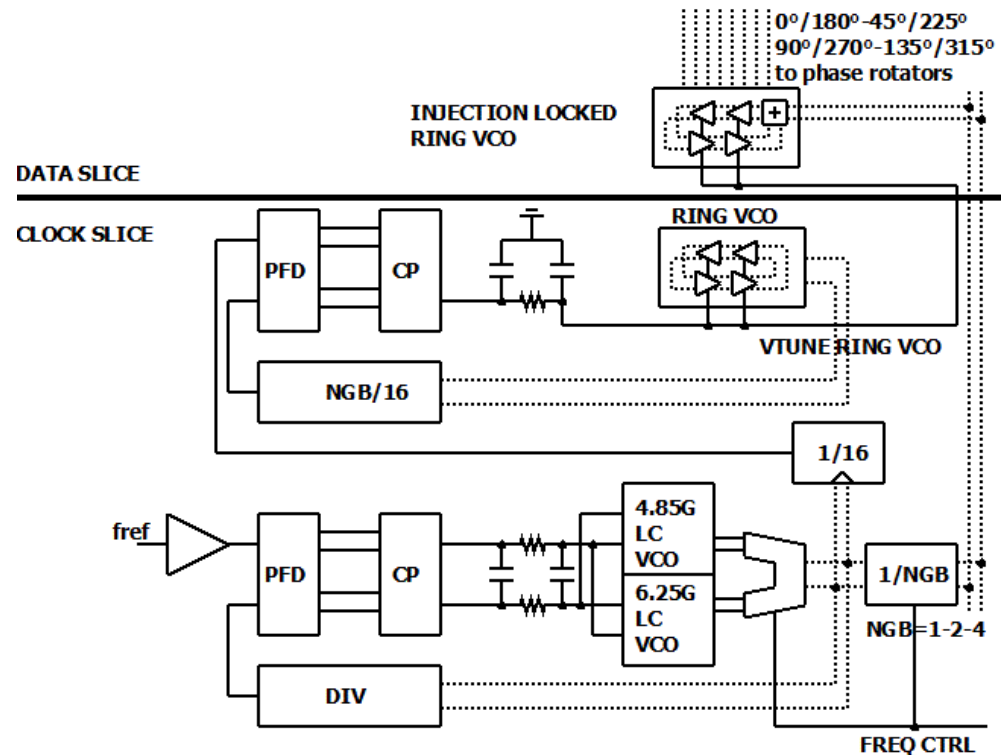
- The full transceiver macro consists of one or more TX/RX ports in parallel called data slices receiving a common low jitter high frequency clock running at half of the data rate from a common distribution line.
- This clock bus is fed by a common clock generation slice in charge of synthesizing the high frequency clock from a reference one in the range of 50 to 350MHz.



# Clock Generation and Distribution



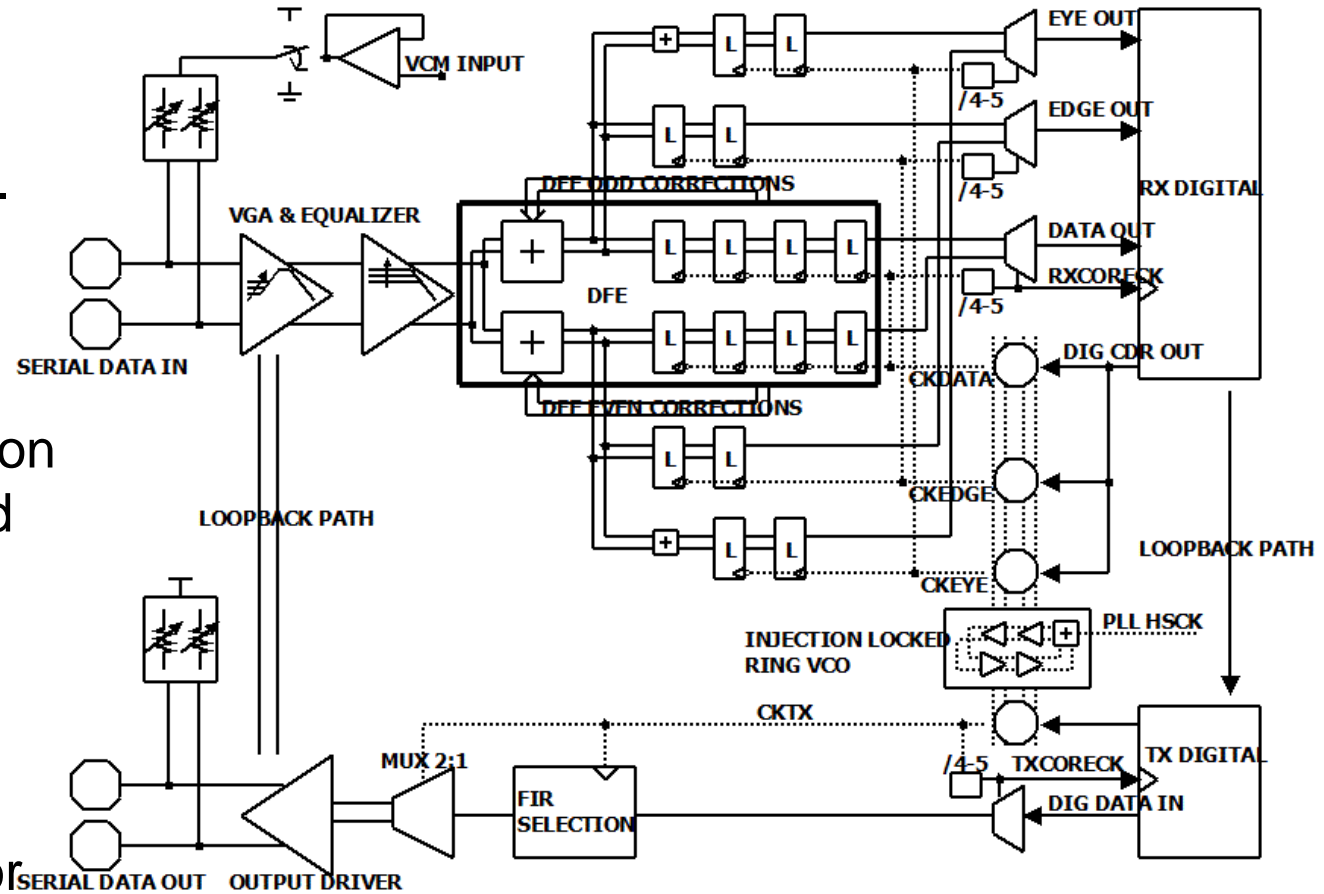
- Two LC VCOs centered respectively at 4.85GHz and 6.25GHz cover a 3.75 to 7.5GHz tuning range:
  - automatic VCO frequency band search to limit the range of the analog tuning voltage.
- 8 phases, required by RX and TX phase interpolators, generated by injection locking the DS 4 stges ring VCO.
- the appropriate control voltage is generated inside the CS through a ring VCO replica closed in a PLL locked to a divided version of the LC PLL HSK.



# Data Slice Overview



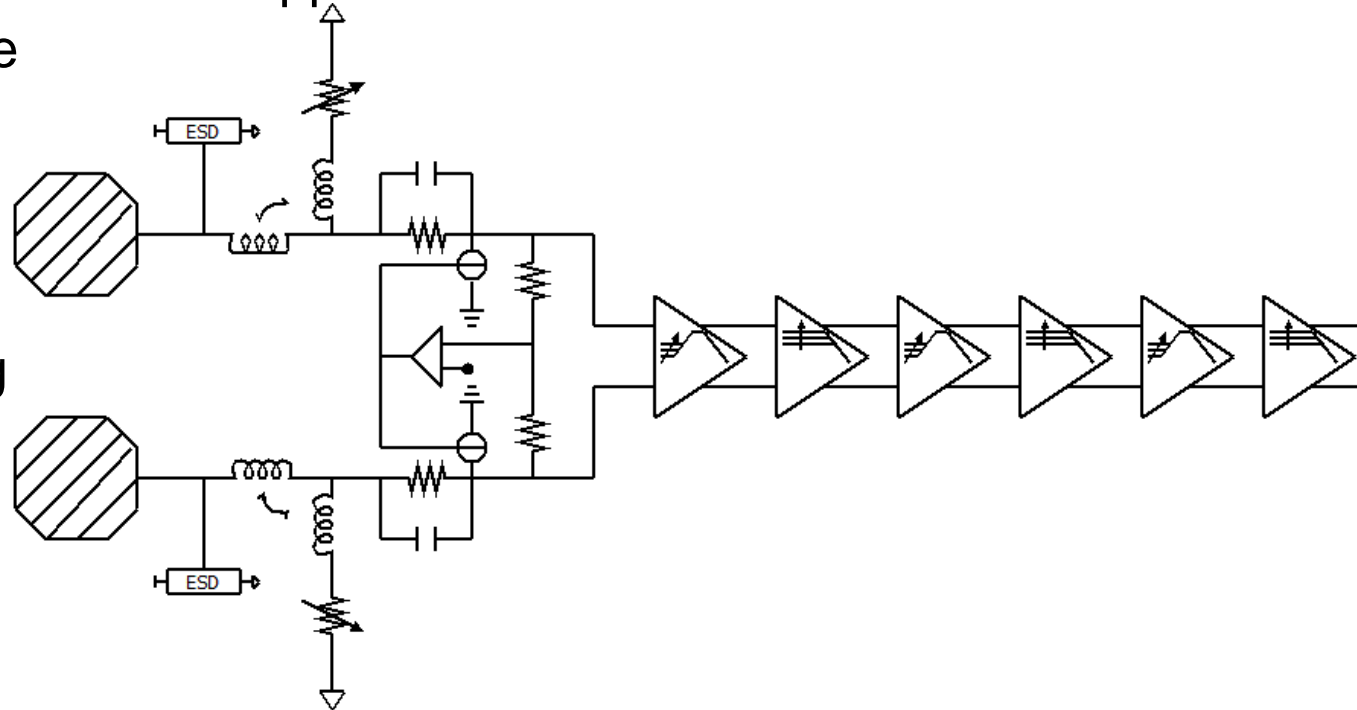
- RX → 1:20 DES.
- RX AFE → signal equalized, re-timed and de-multiplexed.
- RX DIG → clock recovery algorithm, analog blocks calibration-adaptation engine and eye and bathtub analysis.
- TX → 20:1 SER
- FIR logic.
- RX/TX serial and parallel loopback for test and debug.



# Receiver Linear Chain



- Wide band  $100\Omega$  input matching network.
- 0 to 1V accepted input common mode both AC and DC coupling.
- 6 stages analog Feed Forward Equalizer:
  - Programmable DC gain in 8 steps from -4 to 4dB, accepted input data amplitude from 0.4 to 1.2Vppd.
  - Programmable frequency boost in 8 steps from 0 to 16dB at 7GHz peaking frequency.

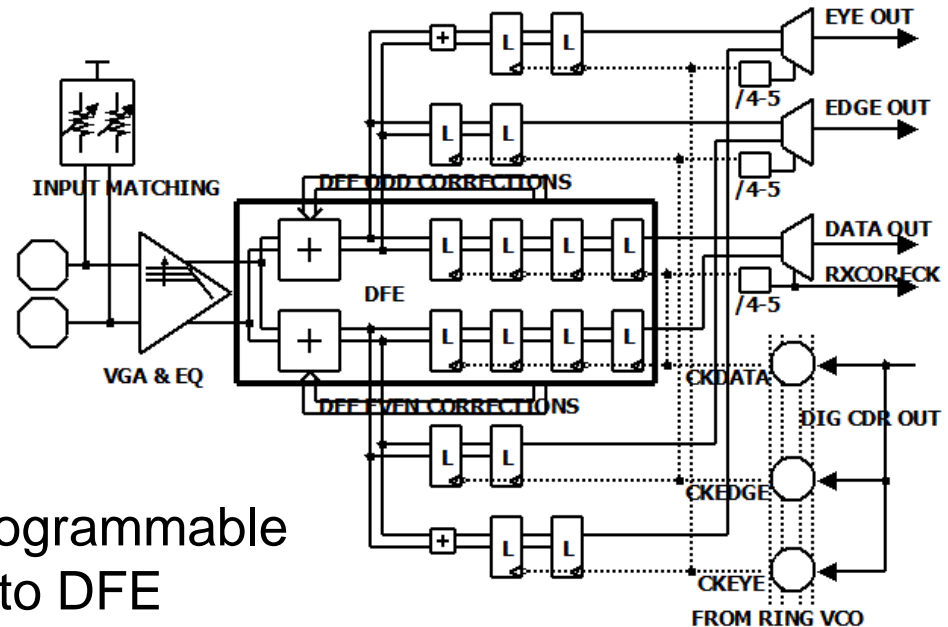


# Clock and Data Recovery Architecture



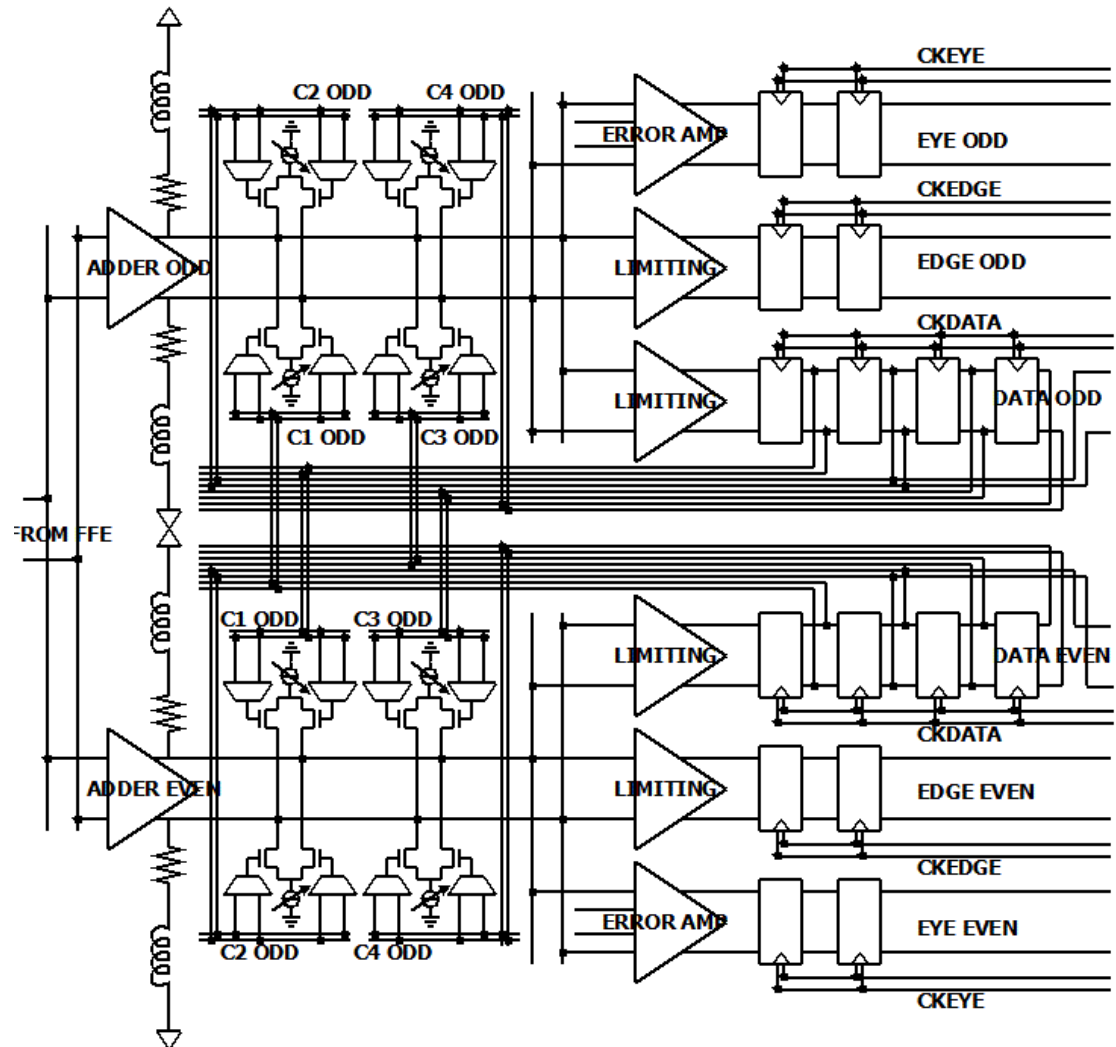
- 3 sampling and de-multiplexing paths

- Primary DATA path in charge of bit decision, provides info to the clock & data recovery.
- 4 taps DFE enhances data recovery equalization capability.
- Clock recovery EDGE path samples data transition and provides info to the clock recovery.
- EYE monitor path: sampler with programmable threshold and phase provides info to DFE adaptation and internal eye monitoring.



# 4 Taps Half Rate DFE

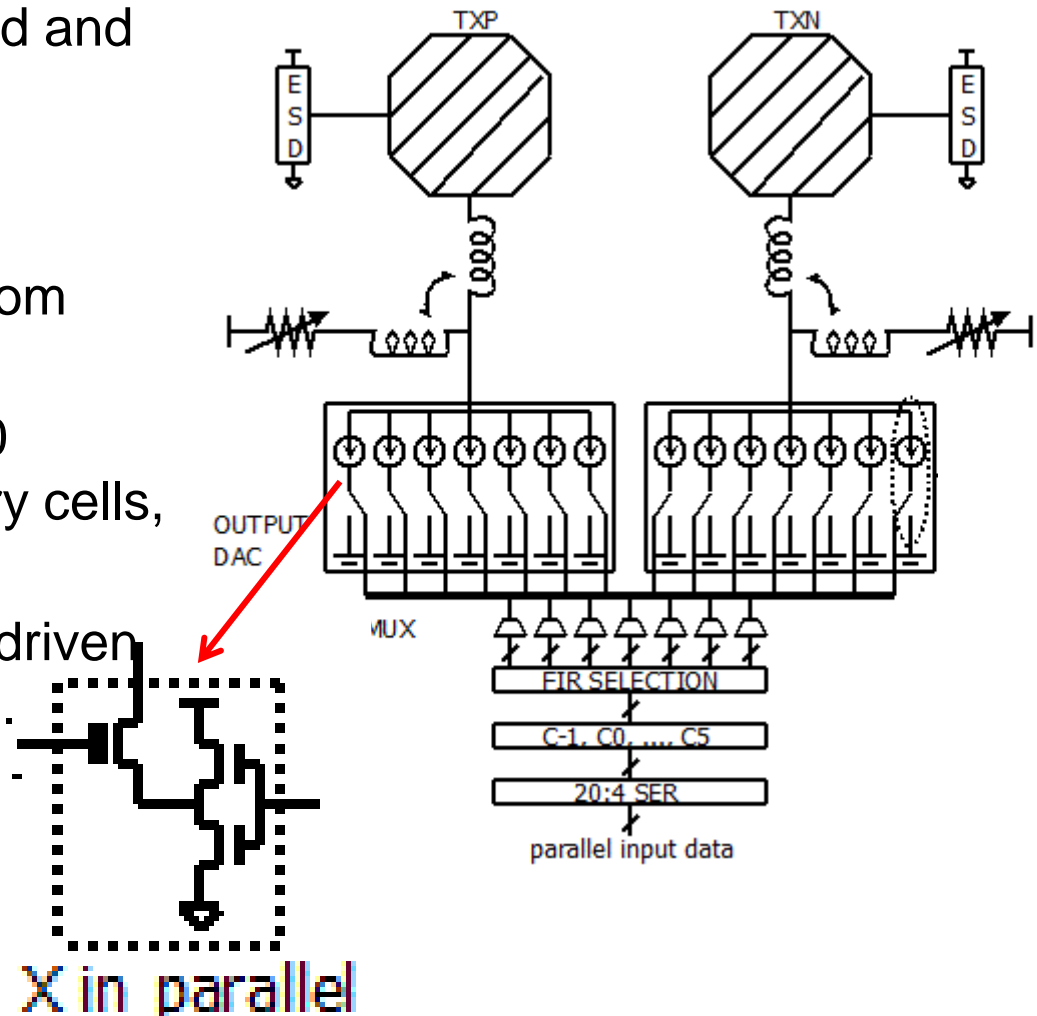
- Half-rate DFE correction: the signal and the corrections summing node split in 2 paths → odd and even bits.
- The 2 paths alternatively provide the DFE corrected bits and transitions to be sampled with the proper edges of CKDATA and CKEDGE.
- Minimum first taps feedback delay by taking them after the first latches.



# Output Driver



- T-coil compensation network to mitigate the effect of the pad and ESD protection parasitic capacitance on return loss.
- The driver amplitude is programmable in 8 steps from 400mV to 1Vppd.
- 5.5mVppd LSB DAC of 180 current-switched elementary cells, divided in 7 groups.
- Each group independently driven by one of the 7 FIR cursors.



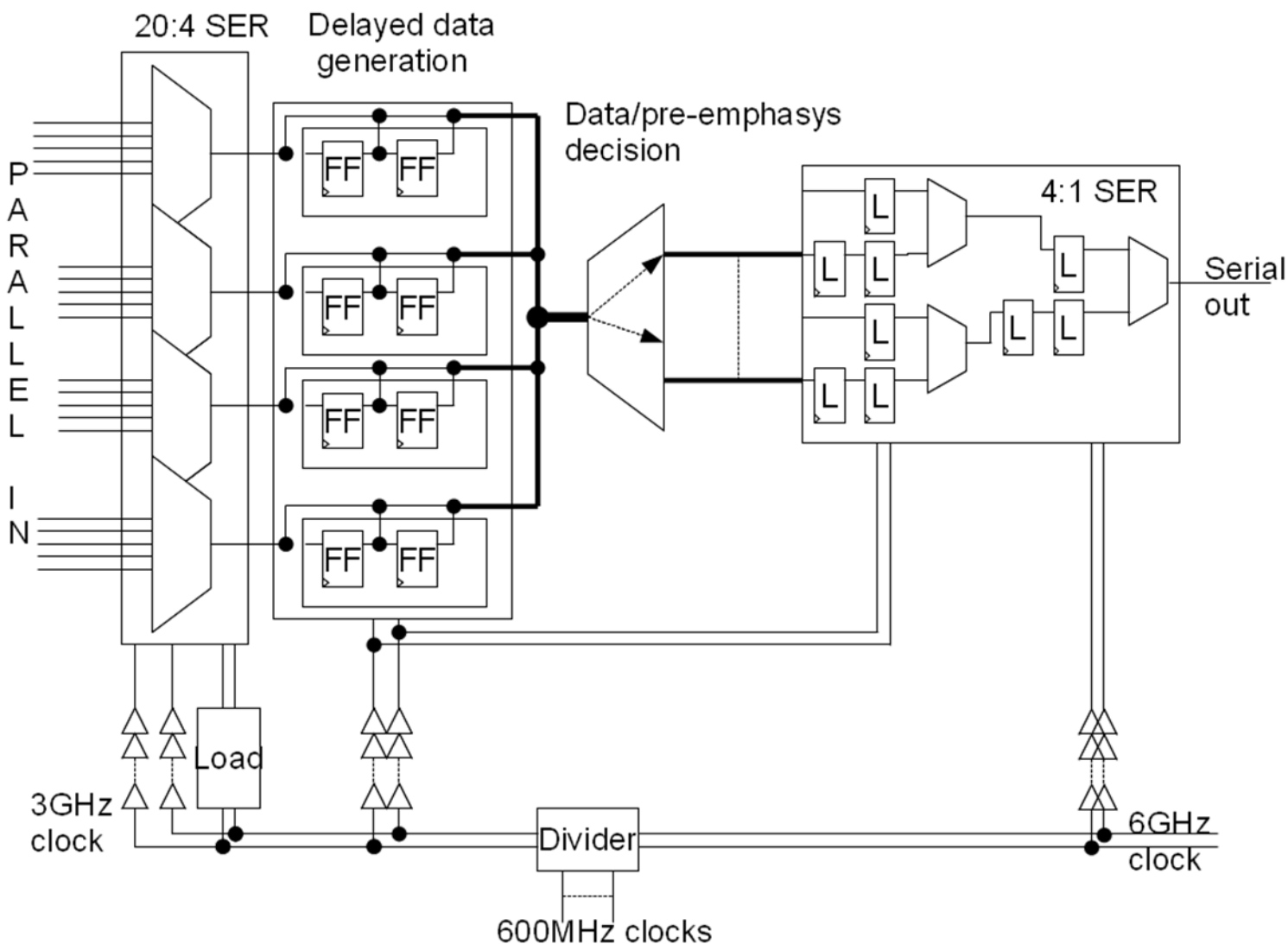
- Highly re-configurable hardware: the groups of elements can be moved from one cursor to the other one according to the maximum allocated weights respecting the limitation of 180 total elementary cells.

Cursor #	C <sub>-1</sub>	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>
Max weight per cursor	15	180	75	45	15	15	15

- Typical 3 taps FIR configuration:
  - Fully compliant to the 802.3ap-KR (10GKR) standard.
  - Up to 9dB of de-emphasis.
  - 350mVppd of minimum DC amplitude.

Cursor #	C <sub>-1</sub>	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>
Typical KR configuration	15	120	45	0	0	0	0

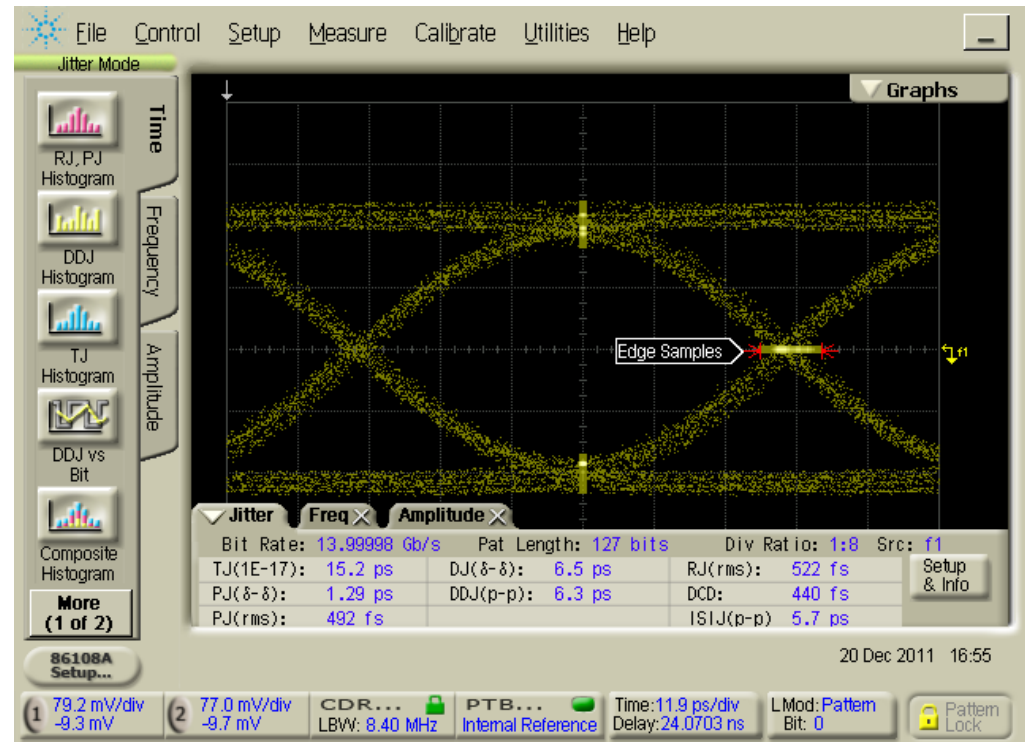
# Serializer Architecture



# Link and Transmitter Performance



- Transmitted eye opening at 14.025Gbit/s after 1.5" FR4:
  - eye aperture 0.8UI
  - eye amplitude 0.8Vppd



- The transceiver operates from 1.25Gbit/s to 14.025Gbit/s, supporting links with more than 22dB channel loss at Nyquist frequency, keeping additional 0.3UI of extrapolated eye opening @ 1E-17 BER measured by the internal bathtub feature.

# Receiver Performance



- Stressed eye analysis @ 14Gbit/s:
  - 18" FR4 channel → 22dB loss at 7GHz
  - 0.3UI of extra jitter injected: 65% random and 35% periodic.

- Sinusoidal jitter tolerance performance VS CEI compliance mask.

