2-Channel 2-Layer Inner-Stack Memory-module Design for LPDDR2/3 DRAM

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Outline

1. Introduction
   1. Mobile Era vs. LPDDR2/3 DRAM
   2. ISM: Inner-Stack Memory-module

2. 2-channel ISM design for LPDDR2/3 using 2-layer PCB
   1. Analysis on Conventional ISM for MDDR
   2. Ideation & Design

3. Simulation Results (Performance)

4. Conclusions
The Explosion of Connected Devices in the Mobile-Era

- Smart Phone
- Ultrabook™ (Laptop)
- Tablet
- Smart TV
- Cloud

"AOAC" must be Guaranteed for Personal Computing in Cloud environment

"Lower STBY" is Mandatory for Always Connected Devices (S.P, Tablet, PC)

Low Standby Current/Power

LPDDR2 & LPDDR3

The continuous synchronization of contents among connected devices is creating better end-user experiences

Courtesy: Samsung EDP Product Planning (2Q'11)
Happiness and Enjoyment in the Mobile World

See

EXPERIENCE = USABILITY/ANALYTIC + DESIGN/CREATIVE

Left

Right

Speech

Text

Numbers

Image

Graphic

Color

&

Enjoy

 Courtesy: Samsung Mobile Product Planning
Mobile DRAM B/W requirement is growing faster.

- MDDR ('05) → LPDDR2 ('10, 2x) → LPDDR3 ('12, 4x)
- High B/W & Density for Graphic & Multimedia performance
  - Graphic resolution increase (1.7x/year) → Bandwidth increment
    - 60fps 5-layer full screen UI for Tablet, 60fps 3-layer full screen UI for S.P
    - 1080P enc/dec, 4X/8X-FSAA, HDR, bigger texture size, continuous shots

Mobile DRAM Bandwidth Requirement

Technology Transition

Wide I/O, LPDDRx

Tablet

0.5GB 1GB 2GB 2GB+

LP1 3.2GB/s LP2 6.4GB/s WUXGA (2560x1600)

2GB+ LP3 12.8GB/s QFHD (3840x2160)

WSVGA (1024x600) WXGA (1280x800)

LPX/WIO

Courtesy: Samsung Mobile Product Planning (2Q‘11)

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## Specification

<table>
<thead>
<tr>
<th>Feature</th>
<th>Item</th>
<th>LPDDR2</th>
<th>LPDDR3</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Item</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CLK frequency</strong></td>
<td></td>
<td>333 / 400 / 533</td>
<td>667 / 800</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td><strong>Max. B/W (1ch / 2ch)</strong></td>
<td></td>
<td>4.25 / 8.5</td>
<td>6.4 / 12.8</td>
<td>GB/s</td>
<td></td>
</tr>
<tr>
<td><strong>CLK/DQS scheme</strong></td>
<td></td>
<td>Differential, Bi-directional</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Data/ADDR/CMD scheme</strong></td>
<td></td>
<td>DDR, Single-ended</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Organization</strong></td>
<td></td>
<td>x16 / x32</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Signaling convention</strong></td>
<td></td>
<td>LVCMOS (&quot;HSUL_12&quot;)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Signaling circuits</strong></td>
<td></td>
<td>• Output: CMOS push-pull driver</td>
<td>• Input: Diff-amp w/external Vref (Data), Full diff-amp (Strobe)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>VDD1/VDD2/VDDQ/VDDCA</td>
<td>1.8 / 1.2 / 1.2 / 1.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Timing Parameter</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>tS / tH</strong></td>
<td></td>
<td>220 / 220</td>
<td>155 / 155</td>
<td>ps</td>
<td>LP2 spec.: 1066Mbps</td>
</tr>
<tr>
<td><strong>tDS / tD</strong></td>
<td></td>
<td>210 / 210</td>
<td>150 / 150</td>
<td>ps</td>
<td>LP3 spec.: 1600Mbps</td>
</tr>
<tr>
<td><strong>tDQSQ / tQHS</strong></td>
<td></td>
<td>200 / 230</td>
<td>145 / 160</td>
<td>pF</td>
<td>On-chip</td>
</tr>
<tr>
<td><strong>Capacitance</strong></td>
<td>CA : 1.0 ~ 2.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>In/Out</strong></td>
<td>DQ : 1.25 ~ 2.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VIH/VIL</strong></td>
<td>VREF +/- 0.22 (AC)</td>
<td>VREF +/- 0.15 (AC)</td>
<td>VREF +/- 0.13 (DC)</td>
<td>V</td>
<td>VREF = 0.5 * VDDQ</td>
</tr>
<tr>
<td><strong>Special Function</strong></td>
<td>PASR, TCSR, Deep Power Down, ZQ Calibration, DQ Calibration</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CA Calibration</strong></td>
<td>N/A</td>
<td>Support</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Write Leveling</strong></td>
<td>N/A</td>
<td>Support</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ODT</strong></td>
<td>N/A</td>
<td>Support *</td>
<td></td>
<td></td>
<td>* VDDQ Term (POD)</td>
</tr>
</tbody>
</table>

**LPDDR3 has little changes from LPDDR2 for easy adoption, only a few functions for 1600Mbps operation**

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Samsung LPDDR2 & 3 give differentiated user experiences

- Higher Performance
- Longer Battery Life
- Smaller & Thinner package solution

Power

Performance

Minimalism

RESPONSIVE

Instant ON → Instant Play

Multi-tasking
Larger screens
Longer Standby

Full HD, 3D

Mobile Computing

Up to 87% of Power Saving during Sleep mode vs. DDR3L

3.7" ≥ 4.0"

Small Size, Small Height

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Challenges in Mobile DRAM Channel

**Mobile Channel Characteristics**

- **P2P w/o Termination (Open term) for lower power consumption**
  - Typical DRAM Channel Length (AP ↔ DRAM) = 10 ~ 50mm
    - Can acts like \( \lambda/4 \) resonator
    - @ 50mm channel: resonance frequency ~ 730MHz
    - It can be checked by evaluating \( Z_{21} \).
  - Small energy couplings can induce large distortions
    - Power Noise can make serious signal integrity issue.

**Combined analysis of SI & PI is important.**

**One of Rep. Measures: Short Channel**

- **PoP**
  - DRAM package on AP/Chipset package
  - Channel in PKG-level (No routing on Board PCB)

- **PiP using ISM**
  - Even shorter channel length is possible.
  - Removal of package-level SMT process

- **Wide I/O (TSV)**
ISM (Inner-Stack Memory Module)

Analysis on Conventional ISM for MDDR

- **1-channel in 12 x 12 mm²**

A PCB design example (117LGA type)

- **Performance**

Chip pad – W/B – PCB trace – Test pad – PCB trace – ISM B/F

Eye @ Test pad

Eye @ Bond Finger

@ 667Mbps
**Design Target (initial)**

- **Supporting LPDDR2 operation in 2-channel:** 800Mbps @ 1.2V
- **Similar Performance/SI:** ISM Bond finger vs. Test pad
- **Chip equivalent size:** 10 x 10 mm² & Low height
  - Alternative to a KGD (known good die)
  - 2 metal-layers PCB with a thin dielectric core

**Key directions**

- **Short routing length**
  - by closing up the test pad to the ISM bond finger
- **Configurational Optimization based on SI/PI**
  - Considering physical limits
    - Conventional Design rules & Assembly processes

This work has been done through 6-sigma process and ideation.
2-channel ISM design for LPDDR2/3

**System Design**

- **Location of ISM Bond finger & Test pad**
  - Edge (fix): ISM bond finger (for wire-bonding & short routing)
  - Central/Inner: Test pad
- **Two types of ISM**
  - Dependent on DRAM chip-shape

**Side-by-Side**
- DQ for Channel 0
- CA for Channel 1
- CA for Channel 0

**Cross-Stacking**
- DQ for Channel 0
- CA for Channel 1
- CA for Channel 0

- 180° rotation
- Rectangular DRAM shape
- 90° rotated vertical stack: Similar to PoP
- Squared DRAM shape

wire-bonding from Chip pad to B/F
**ISM Bond finger configuration**

- **Same order w/ DRAM chip pad**
  - Sig : PWR/GND = 2 : 1
  - DQ side: 83ea & 100um pitch

**Test pad design (I)**

- **Determine Size & Pitch ↔ Securing No. of test pad, Route ability, Testability**
- **Size, Pitch, & No. of Test pads for 2-channel**
  - @ DQ side, ≥ 80ea (≥ 160ea for 2-channel)
    - DQ side is the limiting area.
  - **Simple calculation logic**
    - Considering maximal # of routing lines b/w adjacent test pad: **Round-trip routing**

<table>
<thead>
<tr>
<th>Side-by-Side</th>
<th>Cross-Stacking</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Location of DQ Test pad</strong></td>
<td><strong>Location of DQ Test pad</strong></td>
</tr>
<tr>
<td>PCB Design-rule</td>
<td>PCB Design-rule</td>
</tr>
<tr>
<td>W</td>
<td>W</td>
</tr>
<tr>
<td><strong>Test pad Pitch</strong></td>
<td><strong>Test pad Pitch</strong></td>
</tr>
<tr>
<td>470</td>
<td>450</td>
</tr>
<tr>
<td><strong># of rows</strong></td>
<td><strong># of rows</strong></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td><strong>Half row? (Outer)</strong></td>
<td><strong>Half row? (Outer)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Test pad Size</strong></td>
<td><strong>Test pad Size</strong></td>
</tr>
<tr>
<td>260</td>
<td>240</td>
</tr>
<tr>
<td><strong>Test pad Area</strong></td>
<td><strong>Test pad Area</strong></td>
</tr>
<tr>
<td>8.5 x 8.5 mm x mm</td>
<td>8.2 x 8.2 mm x mm</td>
</tr>
<tr>
<td><strong># of Test pad</strong></td>
<td><strong># of Test pad</strong></td>
</tr>
<tr>
<td>164</td>
<td>160</td>
</tr>
</tbody>
</table>
2-channel ISM design for LPDDR2/3

Test pad design (II)

Test pad: PSR Open size

- Minimal size for Testing
  - 300um (@ Conv. MDDR ISM) → 200um
  - By Real test experiment, 200um is OK!

- To secure ≥ 200um PSR open @ 260um & 240um Test pad metal size
  - Conv. PSR open size @ LGA pad = (Metal size) – (2 x PSR tolerance)
    = 180um, 160um < Too Small >

  - One idea → Widening before the expose of adjacent metal at the maximal offset
    - Test Pad(LGA) of ISM is used for only B/E Testing
    - There is no real connection by Soldering at the test pad → No SJR issue.
    - The test pad is locked by EMC in real application (in PiP).

  - Final (result): 240um & 220um

Test and CI for Two Proportions

<table>
<thead>
<tr>
<th>Sample</th>
<th>X</th>
<th>N</th>
<th>Sample p</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>31360</td>
<td>32000</td>
<td>0.980000</td>
</tr>
<tr>
<td>2</td>
<td>2319</td>
<td>2375</td>
<td>0.976421</td>
</tr>
</tbody>
</table>

Estimate for p(1) - p(2): 0.00357895
95% CI for p(1) - p(2): (-0.00271324, 0.00987113)
Test for p(1) - p(2) = 0 (vs not = 0): Z = 1.11  P-Value = 0.265
2-channel ISM design for LPDDR2/3

2-channel LP2 ISM Bond finger & Test pad Configuration

- **Side-by-Side**
- **Cross-Stacking**

[Diagram showing Side-by-Side and Cross-Stacking configurations for 2-channel LPDDR2/3 memory modules, with details on bond fingers and test pads.]
2-channel ISM design for LPDDR2/3

Performance Compensation b/w ISM B/F & Test pad

- Signal path to ISM B/F > that to Test pad
- Signal performance @ ISM B/F < that @ Test pad

Loop inductance reduction

- Adding bypass PWR/GND Vias close to ISM B/F

Feeding Path 1: from ISM B/F [ @ Real Appl. ]

Feeding Path 2: from Test Pad [ @ Testing ]

Common Path: from Via to Chip pad

Additional (short path) PWR/GND feeding through Vias

\[ L_{\text{Sig}} + L_{\text{PWR/GND}} - 2 \times L_{\text{Mutual}} \]

by reducing this
2-channel ISM design for LPDDR2/3

Design Results: Real PCB Artwork

Top layer

Side-by-Side
Symmetric design b/w Channel 0 & 1

Cross-Stacking

Bottom layer

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**SI/PI Co-simulation for Performance Pre-evaluation**

- **Used simulation schematic [DRAM READ]**
  - w/ combined models of Signal & PWR/GND

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**Simulation Results**

**ISM model (S-para. / Spice)**

**Chipset / AP PKG model (S-para. / Spice)**


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### Simulation Results

#### 800Mbps DQ operation @ Side-by-Side configuration
- 800Mbps: IO speed originally targeted

<table>
<thead>
<tr>
<th>DQ Eyes</th>
<th>ISM Bond Finger</th>
<th>Test Pad</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulated Waveforms w/ 60Ω Driver Strength</td>
<td><img src="image1.png" alt="Waveform Images" /></td>
<td><img src="image2.png" alt="Waveform Images" /></td>
</tr>
<tr>
<td><img src="image3.png" alt="Waveform Images" /></td>
<td><img src="image4.png" alt="Waveform Images" /></td>
<td><img src="image5.png" alt="Waveform Images" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>82 %</td>
<td>78 %</td>
<td>82 %</td>
<td></td>
<td></td>
<td></td>
<td>82 %</td>
<td>78 %</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.03 V</td>
<td>0.03 V</td>
<td>0.03 V</td>
<td></td>
<td></td>
<td></td>
<td>0.03 V</td>
<td>0.03 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>50 ps</td>
<td>70 ps</td>
<td>40 ps</td>
<td></td>
<td></td>
<td></td>
<td>70 ps</td>
<td>70 ps</td>
</tr>
</tbody>
</table>

- **Well operating @ 800Mbps**
  - Negligible difference between through ISM B/F & through Test pad

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### Further evaluation (I) @ LPDDR2 1066Mbps

- Operating
- for the worst byte, AP model was changed

<table>
<thead>
<tr>
<th>Side-by-Side</th>
<th>40Ω D/S (default)</th>
<th>48Ω D/S</th>
<th>60Ω D/S (@ Slow/Slow)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DQ's</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Simulated</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Waveforms</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test Pad</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>SUM</strong></th>
<th>ISM B/F</th>
<th>Test pad</th>
<th>ISM B/F</th>
<th>Test pad</th>
<th>ISM B/F</th>
<th>Test pad</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valid Window</td>
<td>70.8%</td>
<td>70.2%</td>
<td>69.1%</td>
<td>68.5%</td>
<td>57.8%</td>
<td>57.5%</td>
</tr>
<tr>
<td>Overshoot</td>
<td>0.21 V</td>
<td>0.23 V</td>
<td>0.1 V</td>
<td>0.13 V</td>
<td>0.06 V</td>
<td>0.06 V</td>
</tr>
<tr>
<td>Skew</td>
<td>179 ps</td>
<td>185 ps</td>
<td>182 ps</td>
<td>188 ps</td>
<td>249 ps</td>
<td>254 ps</td>
</tr>
</tbody>
</table>

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Further evaluation (II) @ LP2 1066Mbps → Operating (Better)

- for the worst byte, w/ changed AP model

<table>
<thead>
<tr>
<th>Cross-Stack</th>
<th>40Ω D/S (default)</th>
<th>48Ω D/S</th>
<th>60Ω D/S (@ Slow/Slow)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ’s Simulated Waveforms</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test Pad</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SUM</th>
<th>ISM B/F</th>
<th>Test pad</th>
<th>ISM B/F</th>
<th>Test pad</th>
<th>ISM B/F</th>
<th>Test pad</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valid Window</td>
<td>71.9%</td>
<td>71.7%</td>
<td>70.7%</td>
<td>70.7%</td>
<td>62.1%</td>
<td>61.8%</td>
</tr>
<tr>
<td>Overshoot</td>
<td>0.41 V</td>
<td>0.3 V</td>
<td>0.3 V</td>
<td>0.22 V</td>
<td>0.16 V</td>
<td>0.1 V</td>
</tr>
<tr>
<td>Skew</td>
<td>172 ps</td>
<td>175 ps</td>
<td>175 ps</td>
<td>175 ps</td>
<td>229 ps</td>
<td>231 ps</td>
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</tbody>
</table>
Further evaluation (III) @ LPDDR3 1600Mbps → Operating

for the worst byte, w/ changed AP model

<table>
<thead>
<tr>
<th>Side-by-Side</th>
<th>40Ω D/S (default)</th>
<th>48Ω D/S</th>
<th>60Ω D/S (@ Slow/Slow)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DQ’s Simulated Wave-forms</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISM B/F</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test Pad</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUM</td>
<td>ISM B/F</td>
<td>Test pad</td>
<td>ISM B/F</td>
</tr>
<tr>
<td>Valid Window</td>
<td>72.3%</td>
<td>71.5%</td>
<td>69.6%</td>
</tr>
<tr>
<td>Overshoot</td>
<td>0.42 V</td>
<td>0.52 V</td>
<td>0.47 V</td>
</tr>
<tr>
<td>Skew</td>
<td>124 ps</td>
<td>118 ps</td>
<td>138 ps</td>
</tr>
</tbody>
</table>
I/O performance of the 2-channel 2-layer ISMs for LPDDR2/3

- They showed proper operation @ 800Mbps which is the speed originally designed.
  - In real product of side-by-side configuration, it is actually operating well.
    - Its real thickness is 0.38mm high.

- With the recent AP & DRAM models, they are also properly operational up to 1066Mbps for LPDDR2 and even 1600Mbps for LPDDR3.
  - AP package model: package for PoP
    - Signal properties evaluated at the ISM bond finger are similar to those evaluated at the test pad. [High Fidelity]
    - Driver strength option/selection is also important.
  - On-die de-cap. value of AP (for DRAM I/F) as well as that of DRAM IO PDN also strongly affects to the SI performance in PiP (PoP) structure.
We successfully designed 2-channel LPDDR2/3 ISMs in 10mm x 10mm size with thin 2 metal-layer substrate.

- **In designing** (using conventional design-rules),
  - Location of ISM B/F & Test pad ← chip shape, routing scheme
  - Cal. Logic for matrix/No./size/pitch of test pad ← max. routable lines
  - Selection of unavoidable stub length
  - Test pad PSR opening ← test method, structural properties
  - Loop inductance matching by PWR/GND design

We used a SI/PI co-simulation method for I/O evaluation

- Simulation results showed the ISMs are operational up to 1066Mbps for LPDDR2 and 1600Mbps for LPDDR3.
- Almost same performance at both the ISM bond finger & the Test pad

The schemes devised and applied to the design of the ISMs will be efficiently applicable to the design of cost-effective thin high-performance packages such as PoP & interposers.
More speed. Less energy.

Thank you