SPI2012

More speed. Less energy.

2-Channel 2-Layer Inner-Stack Memory-module Design for LPDDR2/3 DRAM

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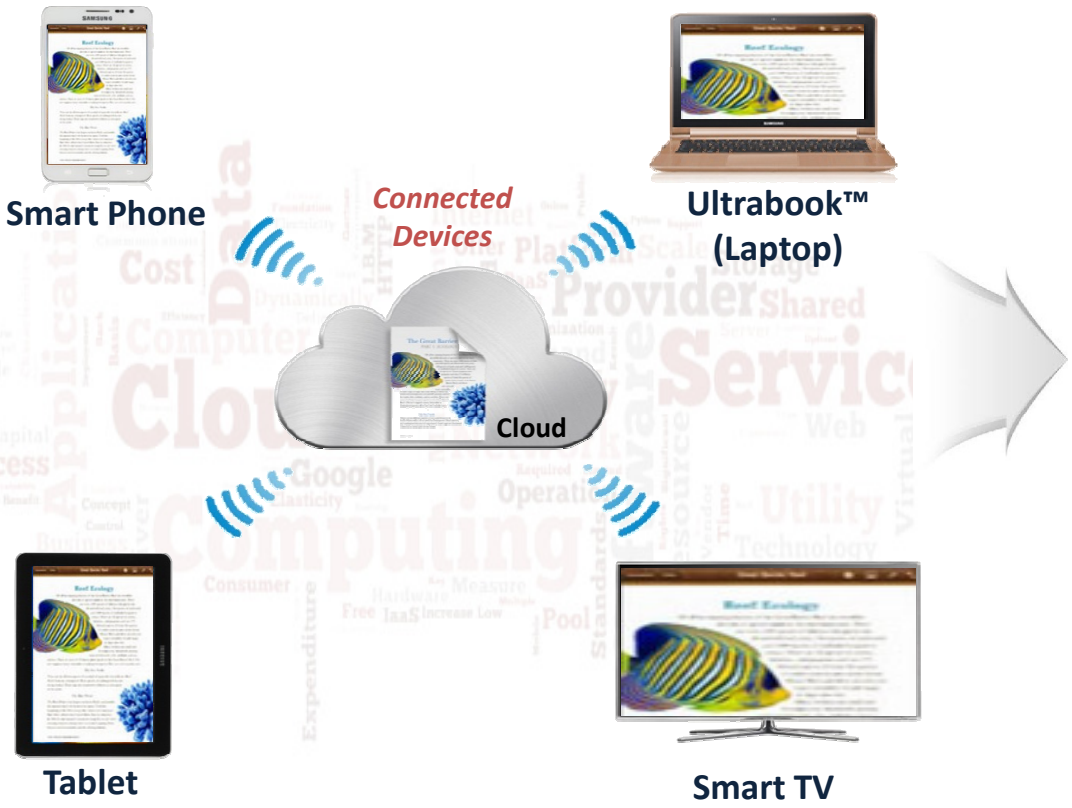
Outline

1. Introduction
    1. Mobile Era vs. LPDDR2/3 DRAM
    2. ISM: Inner-Stack Memory-module
2. 2-channel ISM design for LPDDR2/3 using 2-layer PCB
    1. Analysis on Conventional ISM for MDDR
    2. Ideation & Design
3. Simulation Results (Performance)
4. Conclusions

Mobile Era: Always On, Always Connected

SAMSUNG PROPRIETRY

The Explosion of Connected Devices in the Mobile-Era



"AOAC" must be Guaranteed
for Personal Computing
in Cloud environment

"Lower STBY" is Mandatory
for Always Connected
Devices (S.P, Tablet, PC)

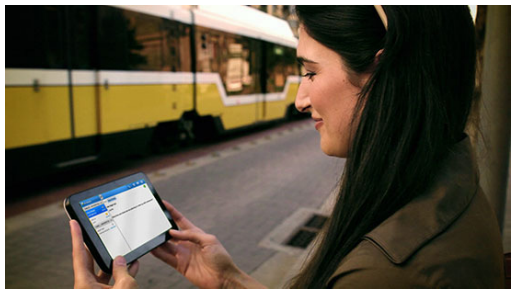
Low Standby Current/Power

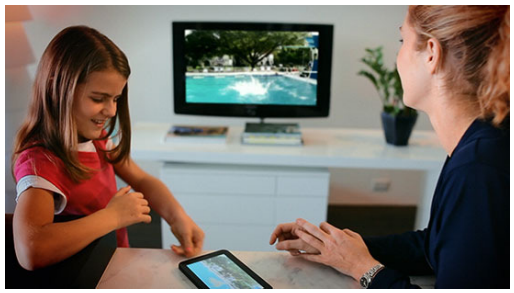
LPDDR2
&
LPDDR3

The continuous synchronization of contents among connected devices is creating better end-user experiences

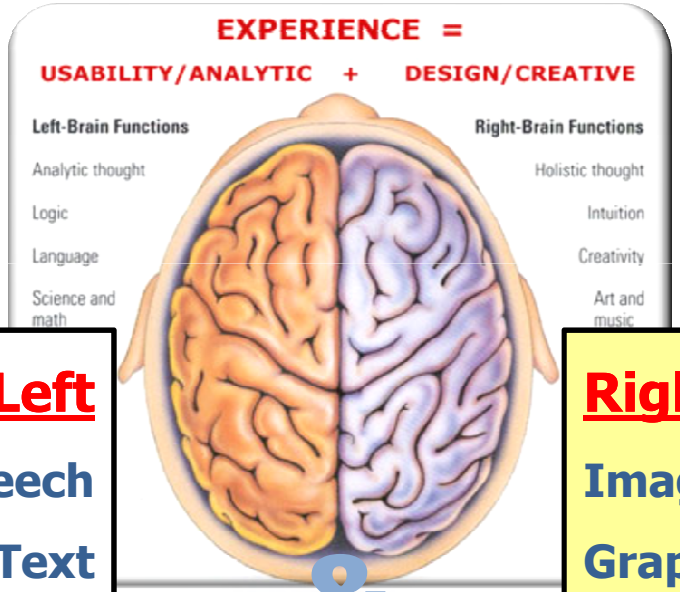
Courtesy: Samsung EDP Product Planning (2Q'11)

Happiness and Enjoyment in the Mobile World





See



Higher Graphic Resolution

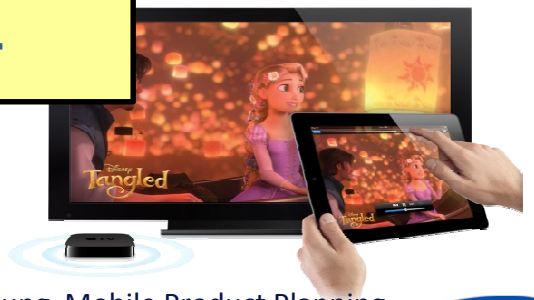
Left
Speech
Text
Numbers

Right
Image
Graphic
Color

Longer Battery Life

&

Enjoy

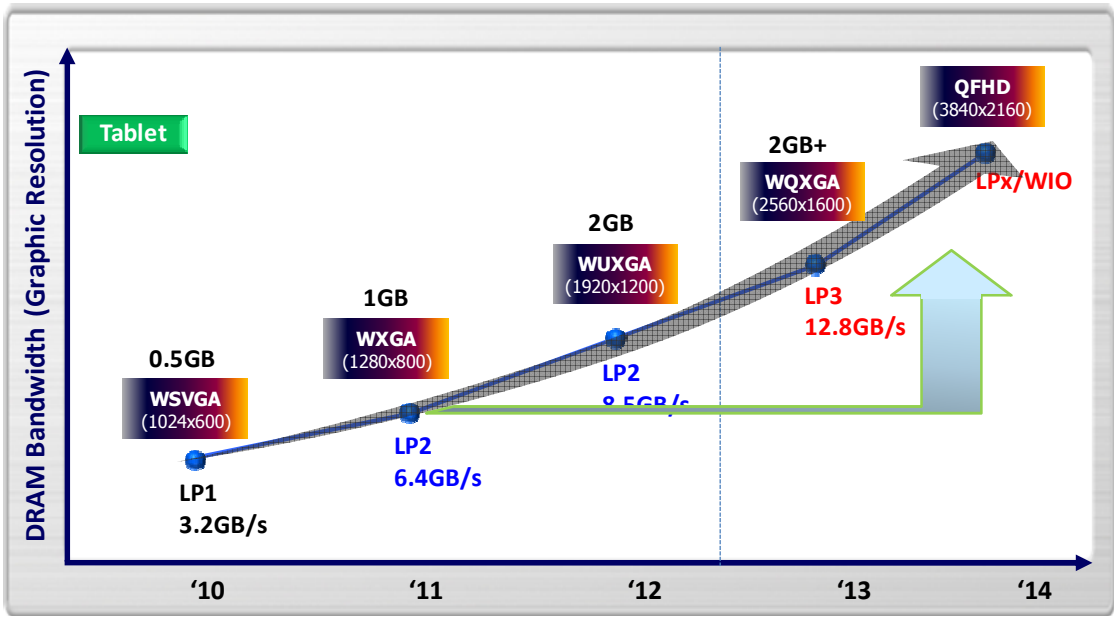


Courtesy: Samsung Mobile Product Planning

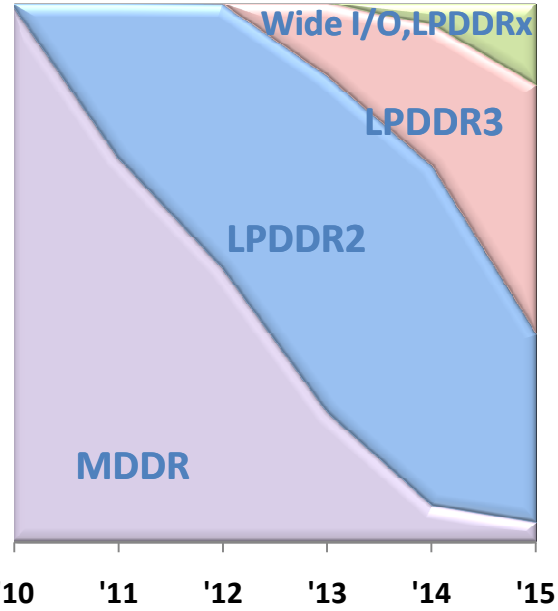
Mobile DRAM Bandwidth Requirement

- **Mobile DRAM B/W requirement is growing faster.**
  - **MDDR ('05) → LPDDR2 ('10, 2x) → LPDDR3 ('12, 4x)**
  - **High B/W & Density for Graphic & Multimedia performance**
    - **Graphic resolution increase (1.7x/year) → Bandwidth increment**
      - 60fps 5-layer full screen UI for Tablet, 60fps 3-layer full screen UI for S.P
      - 1080P enc/dec, 4X/8X-FSAA, HDR, bigger texture size, continuous shots

Mobile DRAM Bandwidth Requirement



Technology Transition



Courtesy: Samsung Mobile Product Planning (2Q'11)

Specification

Item		LPDDR2	LPDDR3	Unit	Remark
Feature	CLK frequency	333 / 400 / 533	667 / 800	MHz	
	Max. B/W (1ch / 2ch)	4.25 / 8.5	6.4 / 12.8	GB/s	
	CLK/DQS scheme	Differential , Bi-directional			
	Data/ADDR/CMD scheme	DDR, Single-ended			
	Organization	x16 / x32			
	Signaling convention	LVCMOS ("HSUL_12")			
	Signaling circuits	• Output: CMOS push-pull driver • Input: Diff-amp w/external Vref (Data), Full diff-amp (Strobe)			
Power	VDD1/VDD2/VDDQ/VDDCA	1.8 / 1.2 / 1.2 / 1.2		V	
Timing Parameter	tIS / tIH tDS / tDH	220 / 220 210 / 210	155 / 155 150 / 150	ps	LP2 spec.: 1066Mbps LP3 spec.: 1600Mbps
	tDQSQ / tQHS	200 / 230	145 / 160	ps	
	In/Out Capacitance	CA : 1.0 ~ 2.0 DQ : 1.25 ~ 2.5	CA : 0.75 ~ 1.5 DQ : 1.0 ~ 2.0	pF	On-chip
	VIH/VIL	VREF +/- 0.22 (AC) VREF +/- 0.13 (DC)	VREF +/- 0.15 (AC) VREF +/- 0.1 (DC)	V	VREF = 0.5 * VDDQ
Special Function	PASR, TCSR, Deep Power Down, ZQ Calibration, DQ Calibration				
	CA Calibration	N/A	Support		
	Write Leveling	N/A	Support		
	ODT	N/A	Support *		* VDDQ Term (POD)

LPDDR3 has little changes from LPDDR2 for easy adoption, only a few functions for 1600Mbps operation

LPDDR2/3 Value Proposition

- **Samsung LPDDR2 & 3 give differentiated user experiences**
  - **Higher Performance**
  - **Longer Battery Life**
  - **Smaller &Thinner package solution**

Power

Multi-tasking
Larger screens
Longer Standby

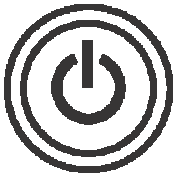
Up to 87% of Power Saving during Sleep mode

vs. DDR3L

Performance

RESPONSIVE

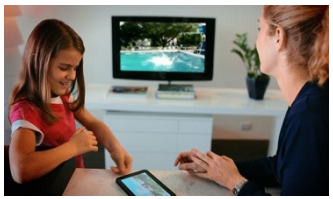
Instant ON → Instant Play



Full HD, 3D

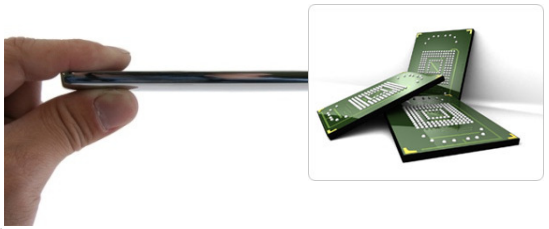
3.7” ≥ 4.0”

Mobile Computing



Minimalism

Small Size, Small Height



Courtesy: Samsung Mobile Product Planning

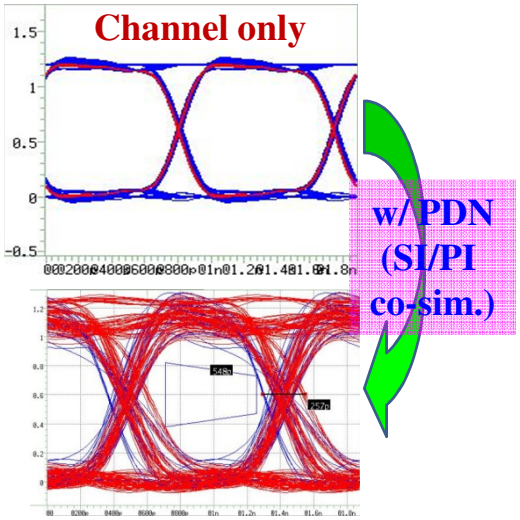
Challenges in Mobile DRAM Channel

Mobile Channel Characteristics

❖ P2P w/o Termination (Open term) for lower power consumption

- **Typical DRAM Channel Length (AP ↔ DRAM) = 10 ~ 50mm**
  - Can acts like $\lambda/4$ resonator
    - @ 50mm channel: resonance frequency ~ 730MHz
      - » It can be checked by evaluating Z_{21}.
- **Small energy couplings can induce large distortions**
  - Power Noise can make serious signal integrity issue.

Combined analysis of SI & PI is important.



One of Rep. Measures: Short Channel

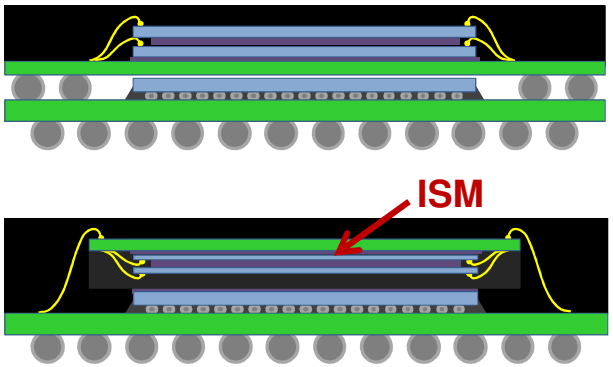
❖ PoP

- DRAM package on AP/Chipset package
- Channel in PKG-level (No routing on Board PCB)

❖ PiP using ISM

- Even shorter channel length is possible.
- Removal of package-level SMT process

❖ Wide I/O (TSV)

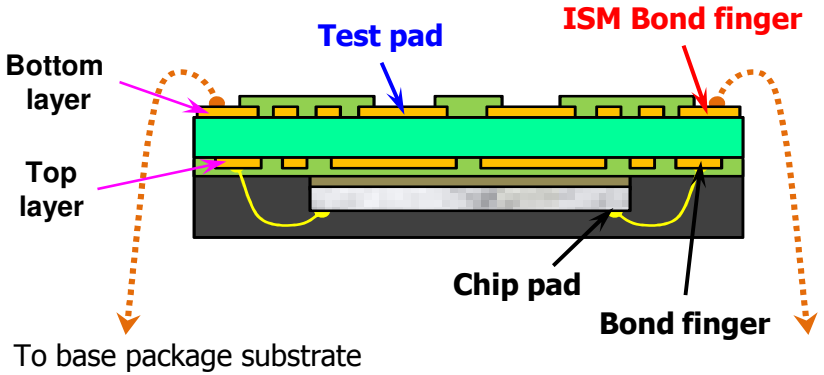


SAMSUNG

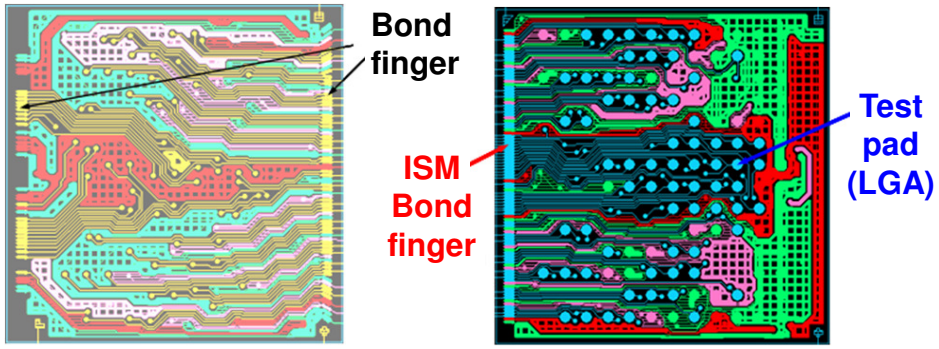
ISM (Inner-Stack Memory Module)

Analysis on Conventional ISM for MDDR

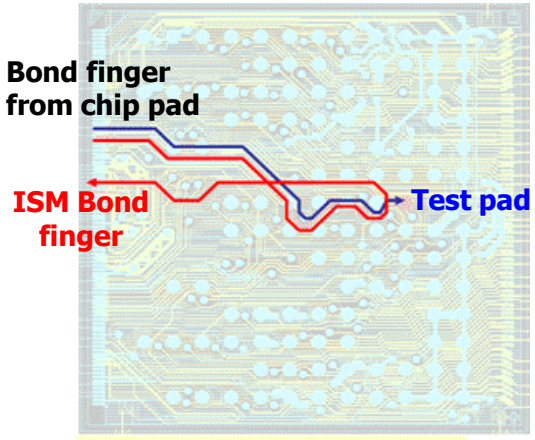
❖ 1-channel in 12 x 12 mm²



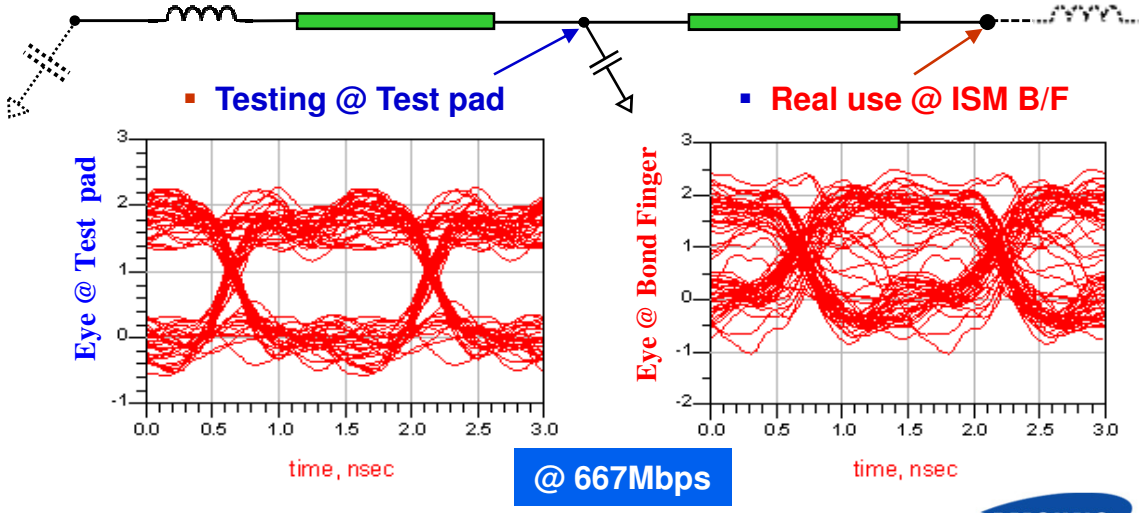
A PCB design example (117LGA type)



❖ Performance



➢ Chip pad – W/B – PCB trace – Test pad – PCB trace – ISM B/F



2-channel ISM design for LPDDR2/3

Design Target (initial)

- **Supporting LPDDR2 operation in 2-channel: 800Mbps @ 1.2V**
- **Similar Performance/SI: ISM Bond finger** vs. **Test pad**
- **Chip equivalent size: 10 x 10 mm^2 & Low height**
  - Alternative to a KGD (known good die)
  - 2 metal-layers PCB with a thin dielectric core

Key directions

- **Short routing length**
  - **by closing up the test pad to the ISM bond finger**
- **Configurational Optimization based on SI/PI**
  - **Considering physical limits**
    - Conventional Design rules & Assembly processes

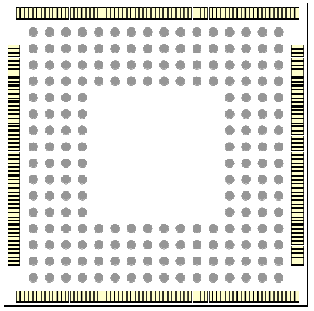
This work has been done through 6-sigma process and ideation.

2-channel ISM design for LPDDR2/3

System Design

❖ Location of ISM Bond finger & Test pad

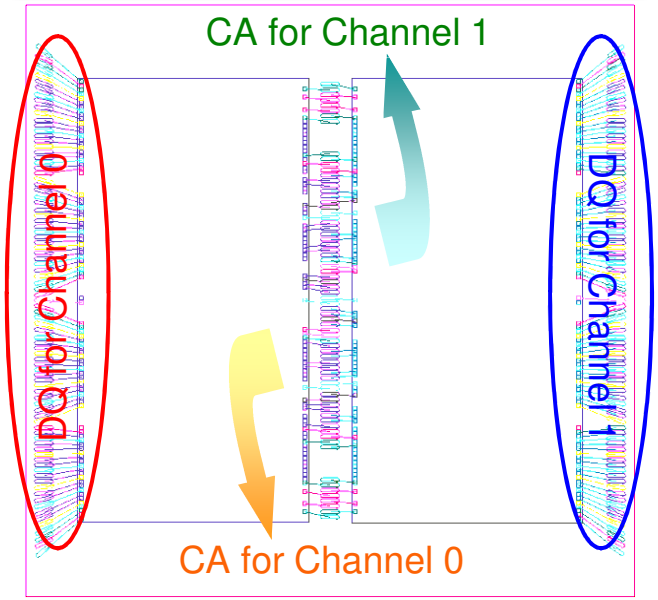
- Edge (fix): ISM bond finger (for wire-bonding & short routing)
- Central/Inner: Test pad



➢ **Two types of ISM**

- Dependent on DRAM chip-shape

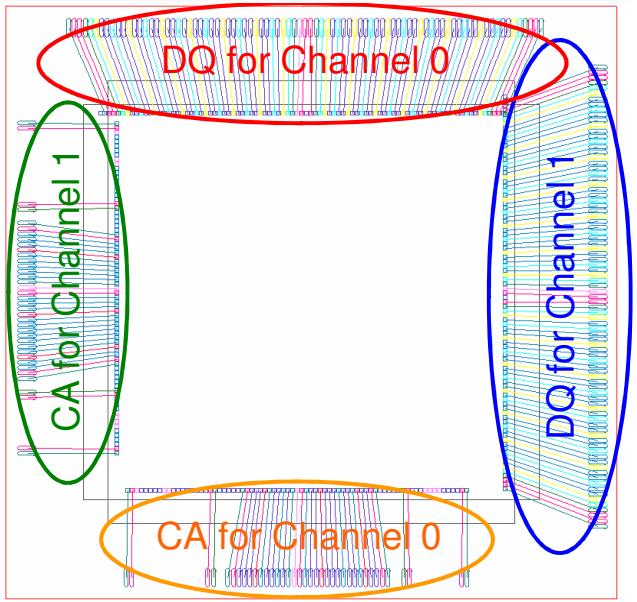
Side-by-Side



[Top]

Wire-bonding from Chip pad to B/F

Cross-Stacking



✓ 180º rotation
✓ Rectangular DRAM shape

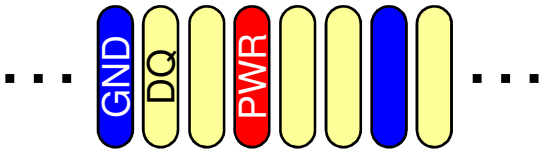
✓ 90º rotated vertical stack: Similar to PoP
✓ Squared DRAM shape

2-channel ISM design for LPDDR2/3

ISM Bond finger configuration

❖ Same order w/ DRAM chip pad

- Sig : PWR/GND = 2 : 1
- DQ side: 83ea & 100um pitch



Test pad design (I)

- **Determine Size & Pitch ← Securing No. of test pad, Route ability, Testability**

❖ Size, Pitch, & No. of Test pads for 2-channel

- **@ DQ side, ≥ 80ea (→ ≥ 160ea for 2-channel)**
  - DQ side is the limiting area.
- **Simple calculation logic**
  - Considering maximal # of routing lines b/w adjacent test pad: Round-trip routing

Side-by-Side

Location of DQ Test pad	Side 1	Side 2	Side 3	Side 4	[unit]
	1	0	1	0	
PCB Design-rule	W	30	S	30	um
Test pad Pitch :	470				um
# of rows :	4				
Half row ? (Outer)	1				
Test pad Size :	260				um
Test pad Area	8.5	x	8.5		mm x mm
# of Test pad	164				ea

Cross-Stacking

Location of DQ Test pad	Side 1	Side 2	Side 3	Side 4	[unit]
	1	1	0	0	
PCB Design-rule	W	30	S	30	um
Test pad Pitch :	450				um
# of rows :	4				
Half row ? (Outer)	1				
Test pad Size :	240				um
Test pad Area	8.2	x	8.2		mm x mm
# of Test pad	160				ea

Test pad design (II)

❖ Test pad: PSR Open size

➢ Minimal size for Testing

- 300um(@ Conv. MDDR ISM) → 200um
- By Real test experiment,

  200um is OK!

Test and CI for Two Proportions

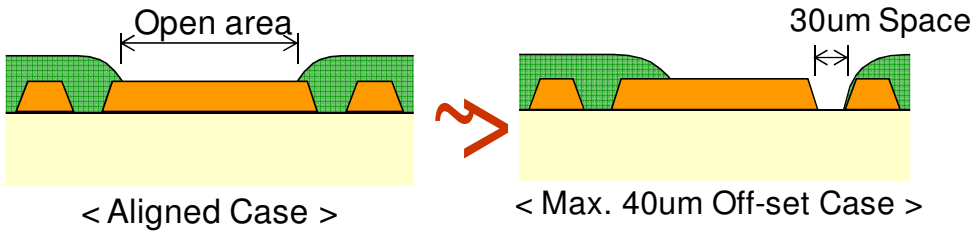
Sample	X	N	Sample p
1	31360	32000	0.980000
2	2319	2375	0.976421

Estimate for p(1) - p(2): 0.00357895
95% CI for p(1) - p(2): (-0.00271324, 0.00987113)
Test for p(1) - p(2) = 0 (vs not = 0): Z = 1.11 **P-Value = 0.265**

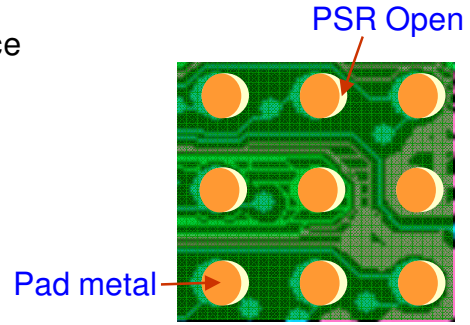
➢ To secure ≥ 200um PSR open @ 260um & 240um Test pad metal size

- Conv. PSR open size @ LGA pad = (Metal size) – (2 x PSR tolerance)
  = 180um, 160um < Too Small >

- One idea ➔ Widening before the expose of adjacent metal at the maximal offset
  - Test Pad(LGA) of ISM is used for only B/E Testing
  - There is no real connection by Soldering at the test pad → No SJR issue.
  - The test pad is locked by EMC in real application (in PiP).



< Aligned Case > < Max. 40um Off-set Case >

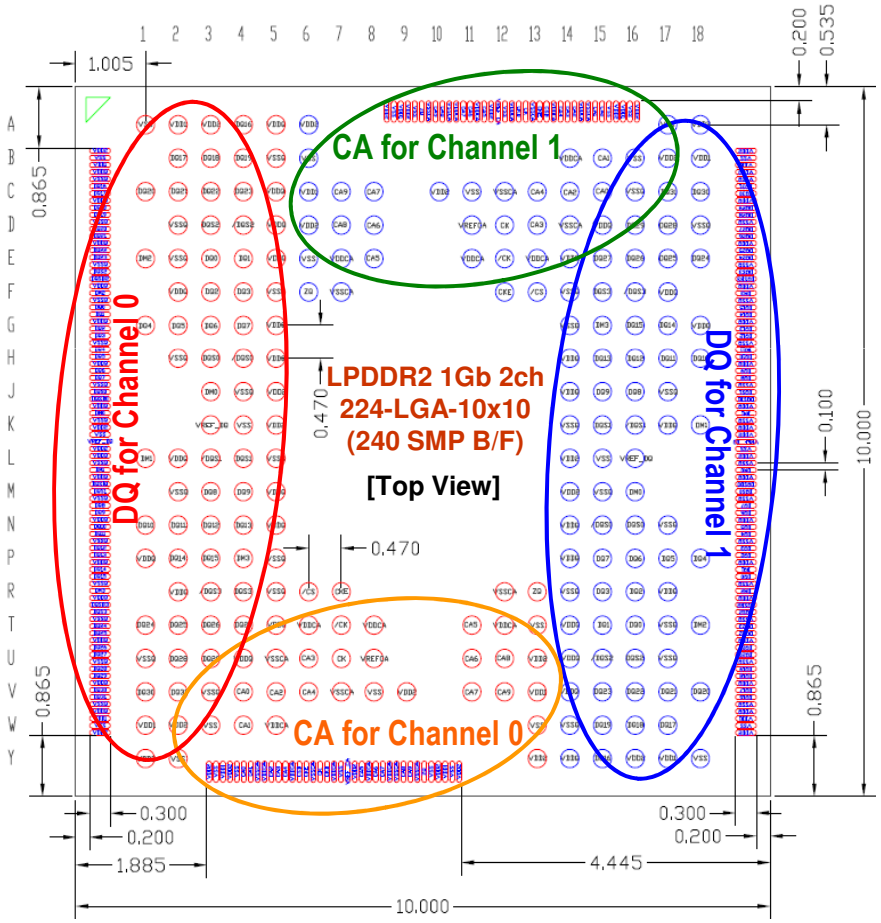


- Final (result): 240um & 220um

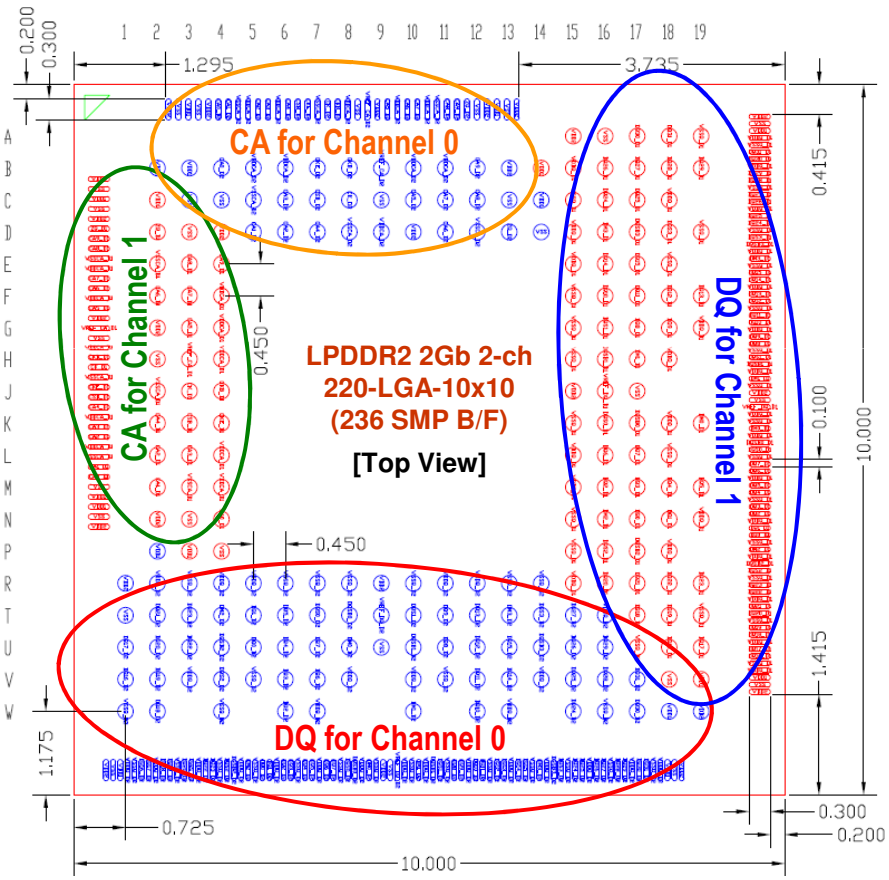
2-channel ISM design for LPDDR2/3

2-channel LP2 ISM Bond finger & Test pad Configuration

Side-by-Side



Cross-Stacking



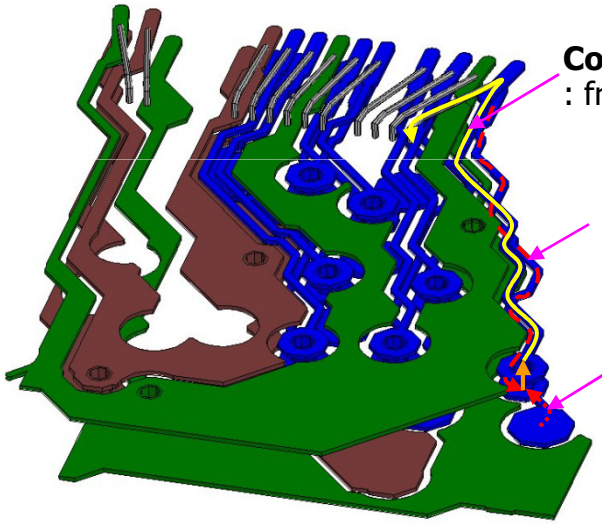
2-channel ISM design for LPDDR2/3

Performance Compensation b/w ISM B/F & Test pad

- Signal path to ISM B/F > that to Test pad
- Signal performance @ ISM B/F < that @ Test pad

Loop inductance reduction

- Adding bypass PWR/GND Vias close to ISM B/F

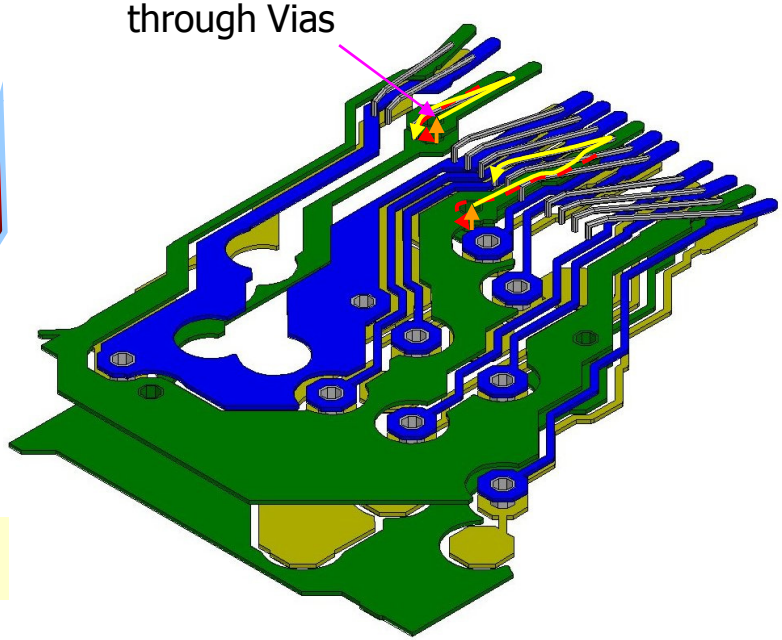


Common Path
: from Via to Chip pad

Feeding Path 1
: from ISM B/F
[@ Real Appl.]

Feeding Path 2
: from Test Pad
[@ Testing]

Additional (short path)
PWR/GND feeding
through Vias

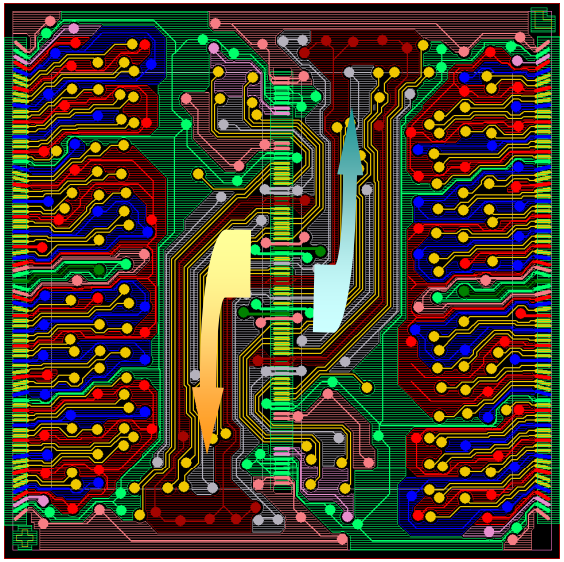


$$L_{Sig} + L_{PWR/GND} - 2 \times L_{Mutual}$$

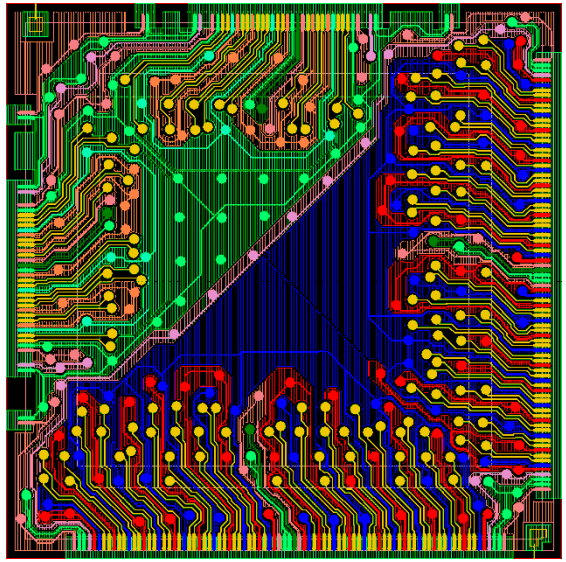
by reducing this

2-channel ISM design for LPDDR2/3

Design Results: Real PCB Artwork

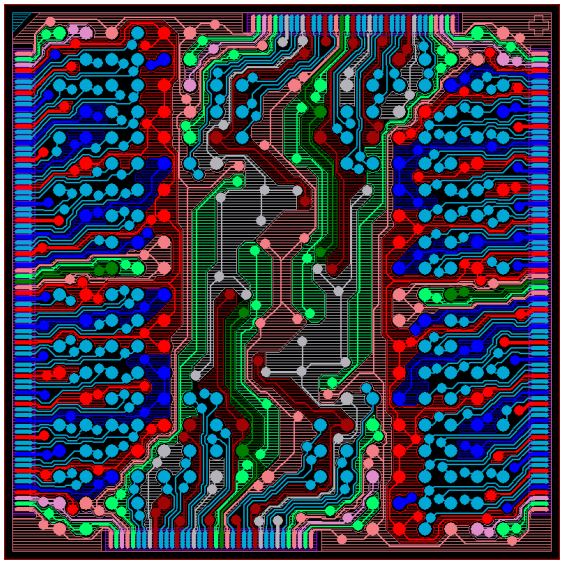


Top layer

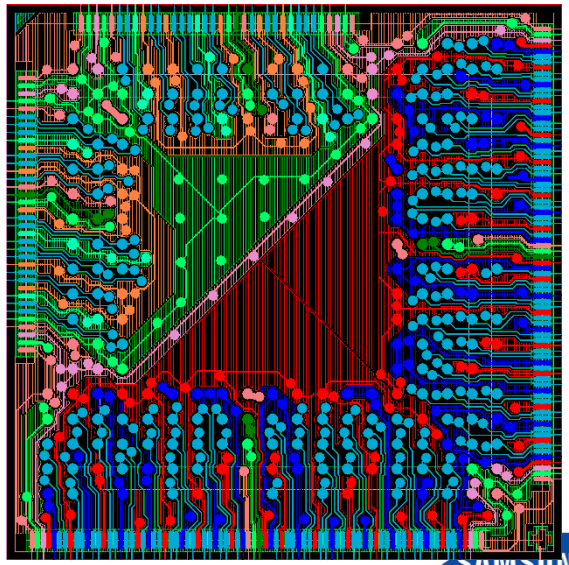


Side-by-Side

Symmetric design
b/w Channel 0 & 1



Cross-Stacking



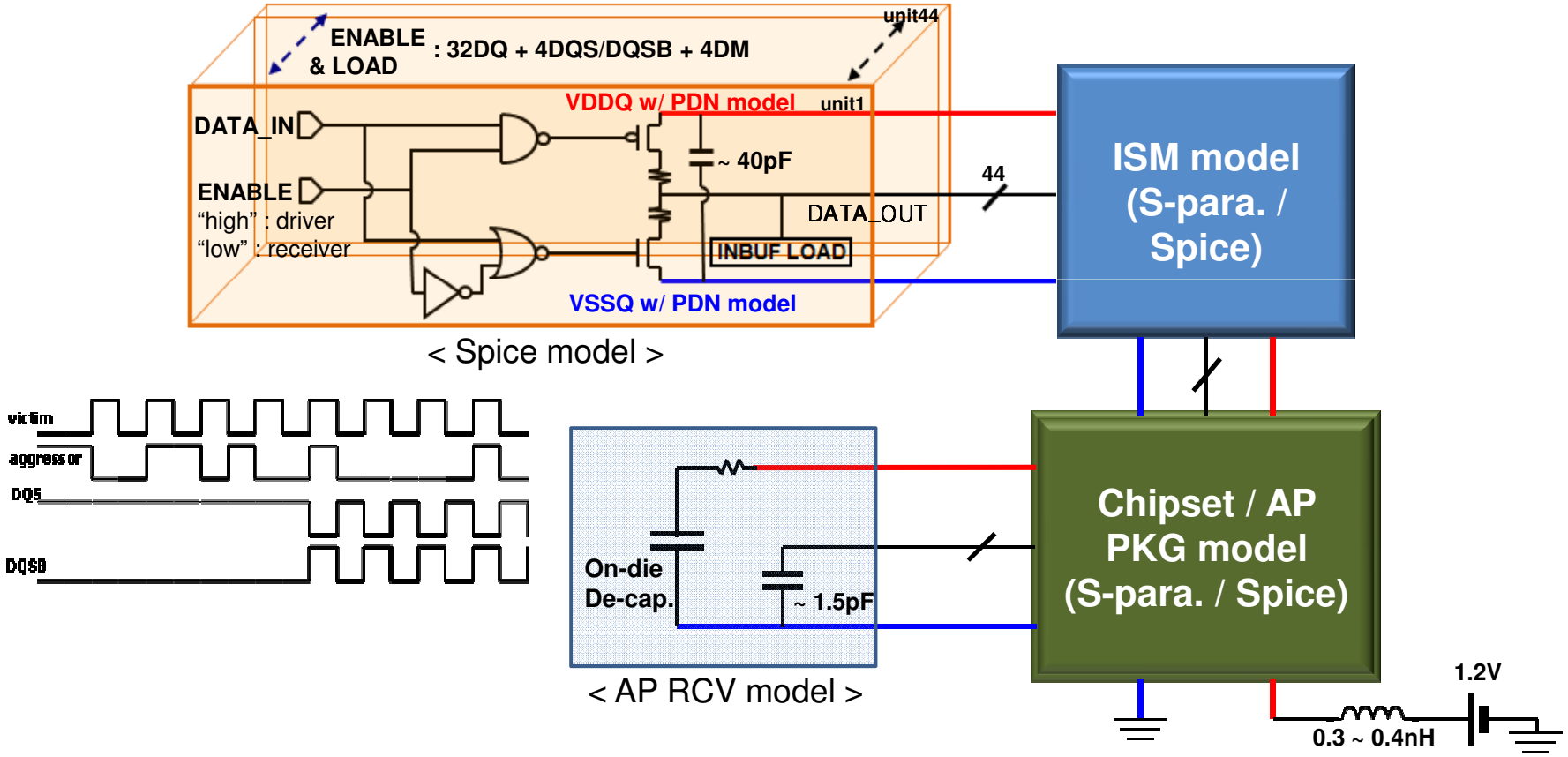
Bottom layer

Simulation Results

SI/PI Co-simulation for Performance Pre-evaluation

❖ Used simulation schematic [DRAM READ]

➢ w/ combined models of Signal & PWR/GND

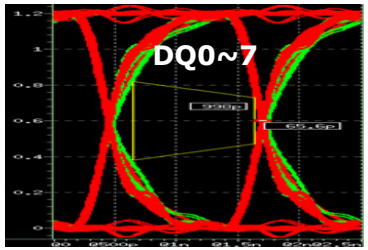
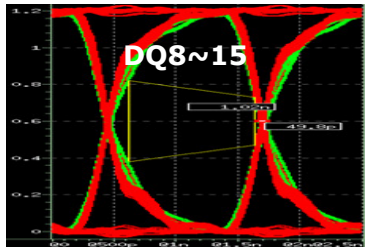
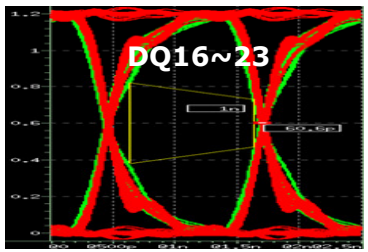
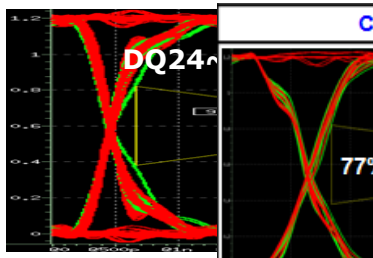
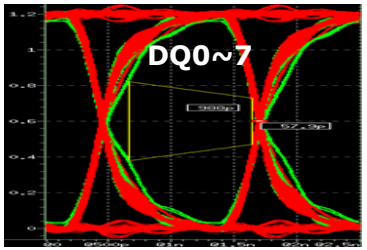
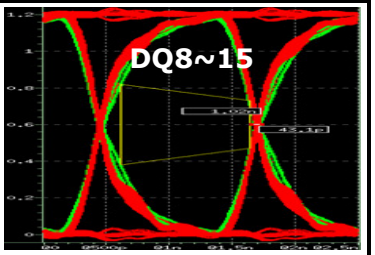
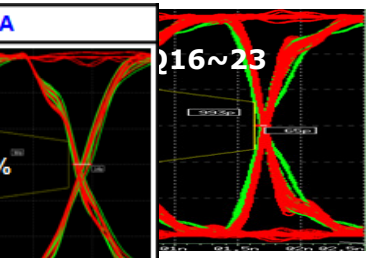
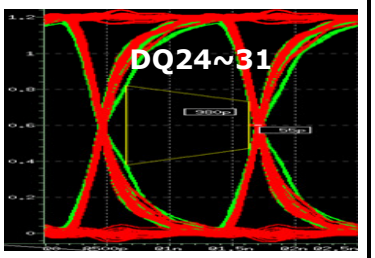


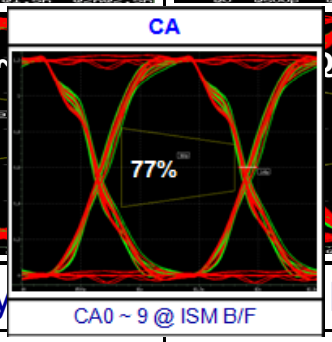
Ref.) Lee, Jongjoo et al, "Split-Ground Effect of Electronic Package on the Input-level of High-speed DRAM," *Proc 53rd ECTC*, 2003, pp. 1440-1444.
Jongjoo Lee, "Effects of Package on the Signal Integrity and Power Integrity of DRAM," EDAPS 2003 Workshop.

Simulation Results

800Mbps DQ operation @ Side-by-Side configuration

- 800Mbps: IO speed originally targeted

DQ Eyes		ISM Bond Finger		Test Pad	
Simulated Waveforms w/ **60Ω** Driver Strength		   		   
SUM	Aperture Ratio	Best byte [1]	Worst by	byte [1]	Worst byte [3]
		82 %	78 %	82 %	78 %
	Overshoot	0.03 V	0.03 V	0.03 V	0.03 V
	Skew	50 ps	70 ps	40 ps	70 ps

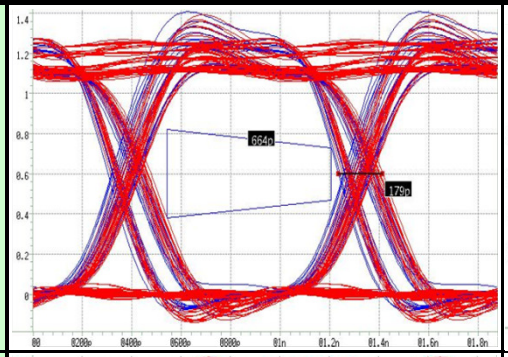
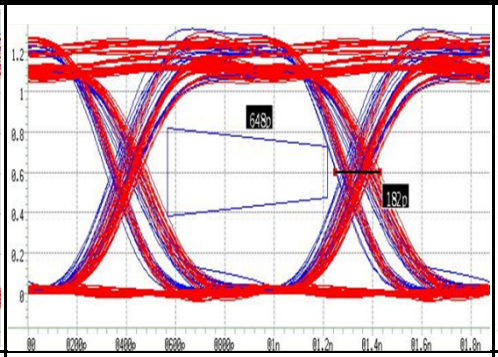
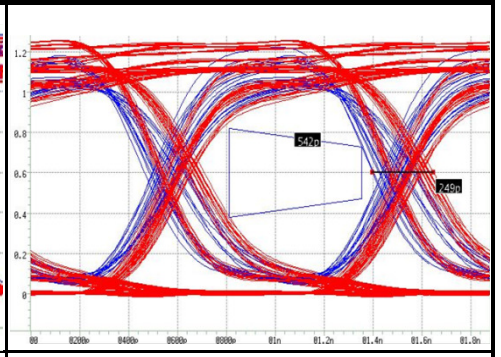
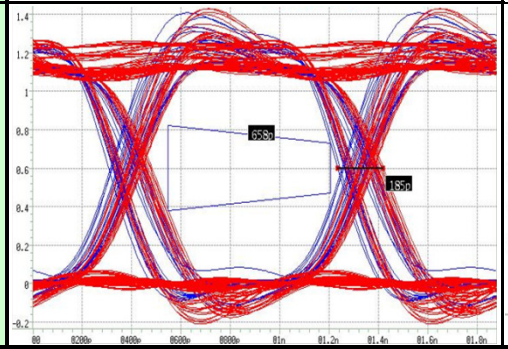
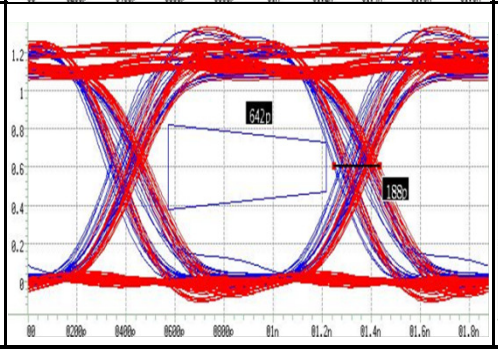
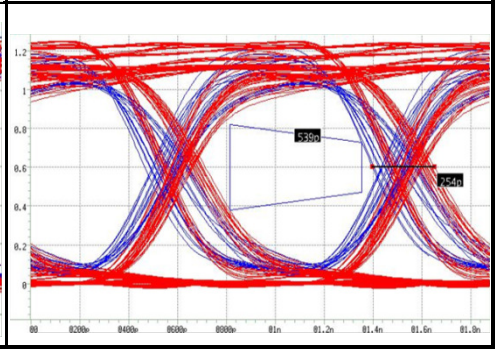


- **Well operating @ 800Mbps**
  - Negligible difference between through ISM B/F & through Test pad

Simulation Results

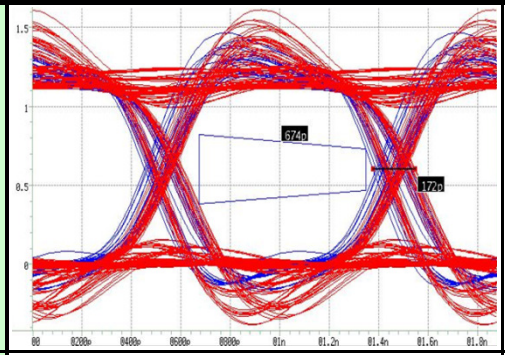
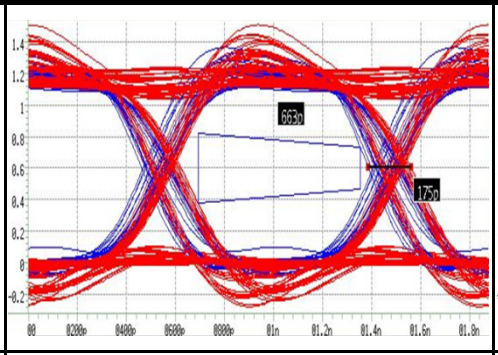
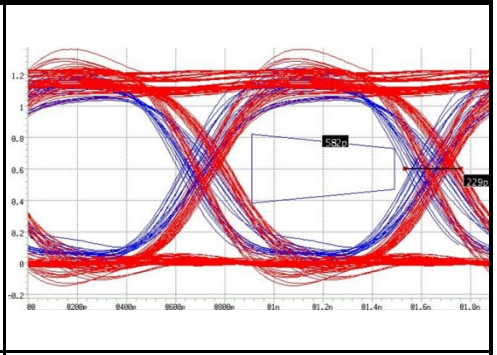
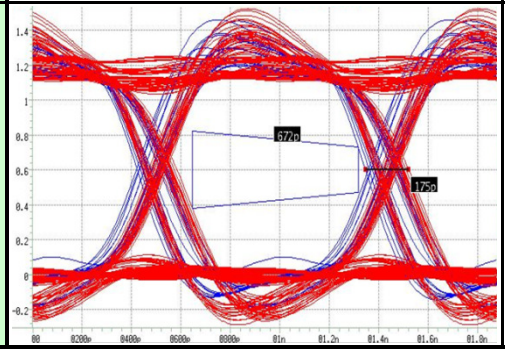
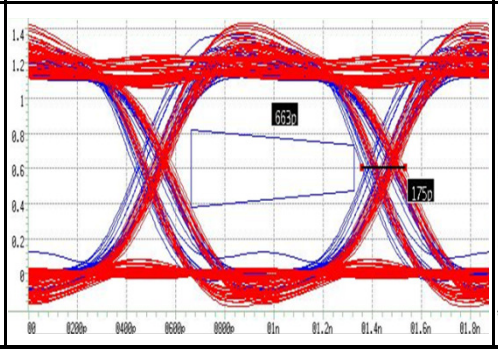
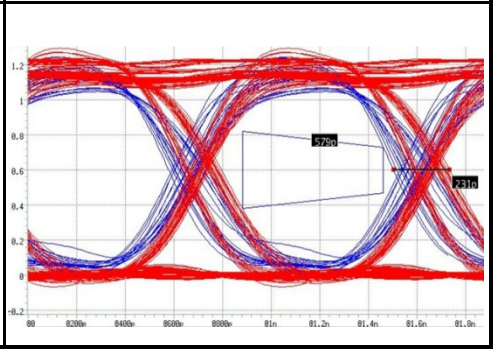
Further evaluation (I) @ LPDDR2 1066Mbps → Operating

- for the worst byte, AP model was changed

Side-by-Side		40Ω D/S (default)		48Ω D/S		60Ω D/S (@ Slow/Slow)	
DQ's Simulated Wave-forms	ISM B/F						
	Test Pad						
SUM		ISM B/F	Test pad	ISM B/F	Test pad	ISM B/F	Test pad
Valid Window		70.8%	70.2%	69.1%	68.5%	57.8%	57.5%
Overshoot		0.21 V	0.23 V	0.1 V	0.13 V	0.06 V	0.06 V
Skew		179 ps	185 ps	182 ps	188 ps	249 ps	254 ps

Simulation Results

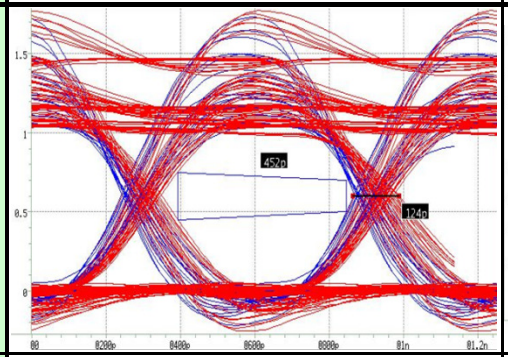
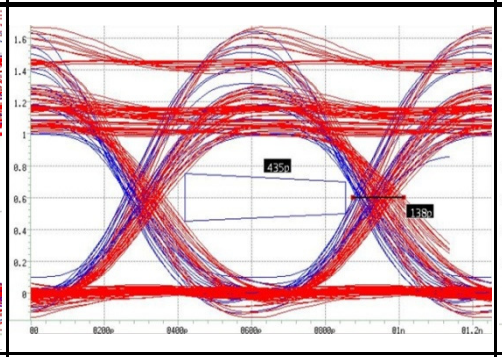
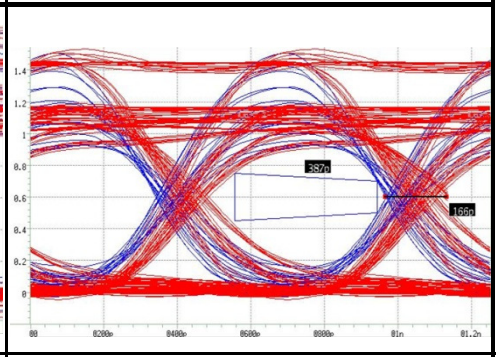
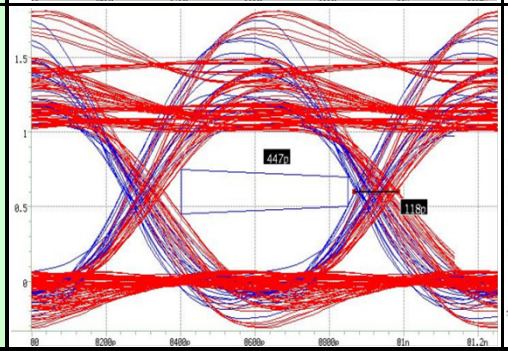
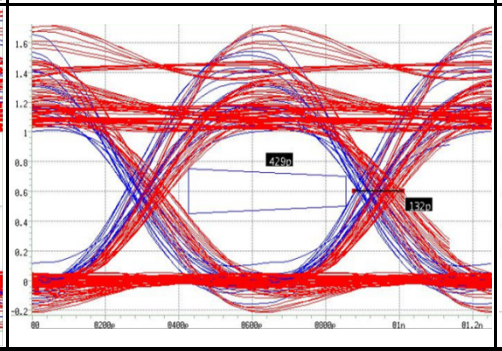
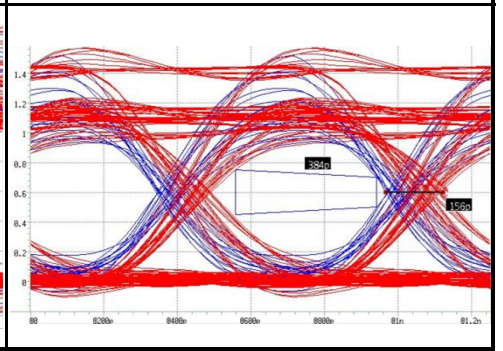
- **Further evaluation (II) @ LP2 1066Mbps → Operating (Better)**
  - for the worst byte, w/ changed AP model

Cross-Stack		40Ω D/S (default)		48Ω D/S		60Ω D/S (@ Slow/Slow)	
DQ's Simulated Wave-forms	ISM B/F						
	Test Pad						
SUM		ISM B/F	Test pad	ISM B/F	Test pad	ISM B/F	Test pad
Valid Window		71.9%	71.7%	70.7%	70.7%	62.1%	61.8%
Overshoot		0.41 V	0.3 V	0.3 V	0.22 V	0.16 V	0.1 V
Skew		172 ps	175 ps	175 ps	175 ps	229 ps	231 ps

Simulation Results

Further evaluation (III) @ LPDDR3 1600Mbps → Operating

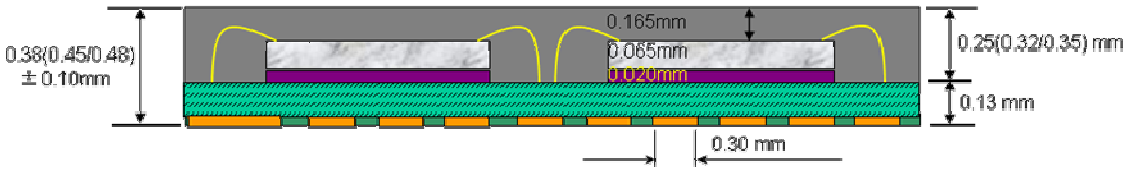
- for the worst byte, w/ changed AP model

Side-by-Side		40Ω D/S (default)		48Ω D/S		60Ω D/S (@ Slow/Slow)	
DQ's Simulated Wave-forms	ISM B/F						
	Test Pad						
SUM		ISM B/F	Test pad	ISM B/F	Test pad	ISM B/F	Test pad
Valid Window		72.3%	71.5%	69.6%	68.6%	61.9%	61.4%
Overshoot		0.42 V	0.52 V	0.47 V	0.5 V	0.33 V	0.37 V
Skew		124 ps	118 ps	138 ps	132 ps	166 ps	156 ps

Summary of Simulation Results

I/O performance of the 2-channel 2-layer ISMs for LPDDR2/3

- **They showed proper operation @ 800Mbps which is the speed originally designed.**
  - **In real product of side-by-side configuration, it is actually operating well.**
    - Its real thickness is 0.38mm high.



- **With the recent AP & DRAM models, they are also properly operational up to 1066Mbps for LPDDR2 and even 1600Mbps for LPDDR3.**
  - AP package model: package for PoP
  - Signal properties evaluated at the ISM bond finger are similar to those evaluated at the test pad. [High Fidelity]
  - Driver strength option/selection is also important.
  - **On-die de-cap. value of AP (for DRAM I/F) as well as that of DRAM IO PDN also strongly affects to the SI performance in PiP (PoP) structure.**

Conclusions

- **We successfully designed 2-channel LPDDR2/3 ISMs in 10mm x 10mm size with thin 2 metal-layer substrate.**
  - **In designing** (using conventional design-rules)**,**
    - Location of ISM B/F & Test pad ←chip shape, routing scheme
    - Cal. Logic for matrix/No./size/pitch of test pad ← max. routable lines
    - Selection of unavoidable stub length
    - Test pad PSR opening ← test method, structural properties
    - Loop inductance matching by PWR/GND design
- **We used a SI/PI co-simulation method for I/O evaluation**
  - **Simulation results showed the ISMs are operational up to 1066Mbps for LPDDR2 and 1600Mbps for LPDDR3.**
  - **Almost same performance at both the ISM bond finger & the Test pad**
- **The schemes devised and applied to the design of the ISMs will be efficiently applicable to the design of cost-effective thin high-performance packages such as PoP & interposers.**


More speed. Less energy.
Thank you
SAMSUNG