

16th Workshop on Signal and Power Integrity

Sorrento, Italy, 13-16 May 2012



Signal Integrity Analysis of Carbon-Based On-chip Nano-Interconnects

Andrea G. Chiariello DII Seconda Università di Napoli ITALY

Antonio Maffucci

DIEI Università di Cassino e del Lazio Meridionale ITALY Giovanni Miano DIEL Università di Napoli Federico II ITALY











Outline

- Challenges for nano-interconnects
- Carbon-nanotubes and graphene nanoribbons
- Circuit models for CNT and GNTs interconnects
- Comparative study of electrical performance of on-chip interconnects
- Conclusions

Projects & acknowledgments

- Nano carbon based components and materials for high frequency electronics (EU-FP7)
- Systems of innovative electronic memories for ICT applications, characterized by high data storage capability and low power dissipation, with convergent architectures and micro and nano integration (EU-PON)





End of the road for Cu interconnects?

Two "electrical" problems for copper nano-interconnects:

Unadequate current carrying capability and maximum allowed current density

Steep increase of Cu resistivity, due to : - barrier scattering, grain boundary scattering, finite barrier layer thickness







Carbon nanotubes and graphene nanoribbon interconnects







Carbon nanotubes, graphene and copper properties

EXPERIMENTAL EVIDENCES







CNT bundles vs multi-layer GNR

	CNT	GNR
Vertical interconnects	Easy	Not available
Horizontal interconnects	Difficult	Easy
Control of fabrication process	Easy	Difficult
Fabrication cost	High	Low
Sensitivity of electrical properties to fabrication process	Low	High





Hybrid CNT+graphene interconnecting structure..



D. Kondo, S. Sato, and Y. Awano,

Self-Organization of Novel Carbon Composite Structure: Graphene Multilayers Combined Perpendicularly with Aligned Carbon Nanotubes

Applied Physics Express, 2008





Real-world examples of successful CMOS-CNT integration..

Pillars made by CNTs bundle CNT pillar bumps for flip-chip high power amplifier







Real-world examples of successful CMOS-CNT integration..

Carbon nanotubes as on-chip interconnects: a 1GHz IC with CNT bundle interconnects wiring CMOS







Real-world examples of successful CMOS-CNT integration..

Carbon nanotubes and graphene on-chip interconnects: CMOS ring oscillator



X. Chen, et al., "Fully Integrated Graphene and Carbon Nanotube Interconnects for Gigahertz High-Speed CMOS Electronics," IEEE Trans. Electr. Devices, 2012





Carbon interconnect modeling: final goal for IC designers







Non-local Ohm law for a generic CNT shell



G. Miano, C. Forestiere, A. Maffucci, S.A. Maksimenko, G. Y. Slepyan, IEEE Trans. on Nanotechnology 2011 and 2012

C. Forestiere, A. Maffucci, G. Miano J. Nanophotonics (2010) Validity limits:

- Low bias conditions $E_z < 0.54 V / \mu m$

- Low frequency

f < 1THz





Transmission line model for an isolated CNT shell or GNR sheet







Transmission line model for CNTs

Typical conditions



 $C'_e \ll C'_O, \quad L'_m \ll L'_k$ $a_C \approx 1, L' \approx L'_k,$ $R' \approx \nu L'_k = \frac{\nu_F}{l_{mfp}} L'_k$ The inductance is **dominated** by the

kinetic term

OK – insensitivity to high-frequency effects (skin and proximity effect)







Impact of the resistance

Resistance model for a single CNT shell or a single GNR



8-888-88	

Bundles of CNTs or arrays of GNRs fed in parallel must be used!!





Circuit model identification: fittings for model parameters

Number of conducting channels:

$$M \approx \begin{cases} 0 & \text{for semicond. SWCNTs} \\ 2 & \text{for metallic SWCNTs} \\ a_1DT + a_2 & \text{for MWCNTs} \end{pmatrix} \\ \frac{M_0(W)}{\alpha - \beta T} & \text{for GNRs} \end{pmatrix}$$

$$rigorously computed in:$$
G. Miano, C. Forestiere, A. Maffucci, S.A. Maksimenko, G. Y. Slepyan, IEEE Trans. on Nanotechnology 2011
C. Xu, H. Li, and K. Banerjee, IEEE Trans. Electron Devices, 2009

Mean free path:



The fitting coefficients depend on the temperature and size ranges





Model validation - CNT







Model validation - GNR







Signal integrity performance of on-chip CNT interconnects



ITRS 2011 Edition

	22 nm node		
	global	interm.	local
W [nm]	160.00	44.00	22.00
H [nm]	96.00	44.00	44.00
Rdr [k Ω]	0.16	0.81	8.09
Cout [fF]	4.90	0.98	0.09
CL [fF]	14.00	2.80	0.28



16th Workshop on Signal and Power Integrity

Sorrento, Italy, 13-16 May 2012



Local level







Intermediate level





16th Workshop on Signal and Power Integrity

Sorrento, Italy, 13-16 May 2012



Intermediate level







Hybrid CNT /GNR/Cu on-chip interconnect







Performance at 1GB/s (400K)







Performance at 5 GB/s (400K)







Performance at 10 GB/s (400K)







Summary: electrical performance vs copper interconnects

	Local interconnects	Global interconnects	On-chip Vias	Chip-to-package interconnects
SWCNT	Comparable or better (depending on the metallic fraction)	Comparable or better (depending on the metallic fraction)	Comparable or better (depending on the metallic fraction)	Comparable or better (depending on the metallic fraction)
MWCNT	comparable	better	worse	better
GNR	comparable	worse or better (stronlgy depending on the edge effect and doping)	Not available	Not available





Conclusions

- Carbon-based interconnects are proposed to replace copper for on-chip interconnects for technology nodes of 22 nm and below.
- **Carbon nanotubes** and **graphene nanoribbons** are candidate to realize them. First examples of **monolithic CNT/CMOS** and **GNR/CMOS integration**.
- Circuit models for carbon interconnects may be derived in the frame of the TL theory. Besides classical parameters, quantistic terms appear (such as kinetic inductance and quantum capacitance) which strongly affect the electrical behavior.
- A simple model has been proposed and validated, based on fittings of the physical parameters. The fitting formulas are function of temperature and size
- Signal integrity analysis show the potential electrical performance of the proposed solutions, some of them **strongly influenced** by the possibility to have good control in fabrication process



16th Workshop on Signal and Power Integrity

Sorrento, Italy, 13-16 May 2012



Thank you