Signal Integrity Analysis of Carbon-Based On-chip Nano-Interconnects

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A.G. Chiariello, A. Maffucci, G. Miano - Signal Integrity Analysis of Carbon-Based On-chip Nano-Interconnects
Outline

- Challenges for nano-interconnects
- Carbon-nanotubes and graphene nanoribbons
- Circuit models for CNT and GNTs interconnects
- Comparative study of electrical performance of on-chip interconnects
- Conclusions

Projects & acknowledgments

- *Nano carbon based components and materials for high frequency electronics (EU-FP7)*
- *Systems of innovative electronic memories for ICT applications, characterized by high data storage capability and low power dissipation, with convergent architectures and micro and nano integration (EU-PON)*
End of the road for Cu interconnects?

Two “electrical” problems for copper nano-interconnects:

- Steep increase of Cu resistivity, due to:
  - barrier scattering, grain boundary scattering, finite barrier layer thickness
- Unadequate current carrying capability and maximum allowed current density


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Carbon nanotubes and graphene nanoribbon interconnects

Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require **material innovation**, combined with accelerated design, packaging and unconventional interconnects” – ITRS, 2011

- **Single-wall CNT (SWCNT)**
  - Av. diameter: 1-6 nm

- **Multi-wall CNT (MWCNT)**
  - Av. external diameter: 20-50 nm

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Carbon nanotubes, graphene and copper properties

EXPERIMENTAL EVIDENCES

<table>
<thead>
<tr>
<th></th>
<th>Cu</th>
<th>SWCNT</th>
<th>MWCNT</th>
<th>Graphene or GNR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max current density (A/cm²)</td>
<td>$10^7$</td>
<td>$&gt;10^9$</td>
<td>$&gt;10^9$</td>
<td>$&gt;10^8$</td>
</tr>
<tr>
<td>Melting point (K)</td>
<td>1356</td>
<td>3800</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tensile strength (GPa)</td>
<td>0.22</td>
<td>22.2±2.2</td>
<td>11-63</td>
<td></td>
</tr>
<tr>
<td>Thermal conductivity (×10³ W/m-K)</td>
<td>0.385</td>
<td>1.75-5.8</td>
<td>3</td>
<td>3-5</td>
</tr>
<tr>
<td>Temperature Coefficient of Resistance (×10⁻³/K)</td>
<td>4</td>
<td>&lt;1.1</td>
<td>-1.37</td>
<td>-1.47</td>
</tr>
<tr>
<td>Mean free path (nm) @ room temperature</td>
<td>40</td>
<td>$&gt;10^3$</td>
<td>$2.5×10^4$</td>
<td>$1×10^3$</td>
</tr>
</tbody>
</table>

- higher current density
- better heat removal
- stability of resistance with temperature (TCR may be even <0)
- Ballistic transport (zero resistance) for longer distances

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### CNT bundles vs multi-layer GNR

<table>
<thead>
<tr>
<th></th>
<th>CNT</th>
<th>GNR</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Vertical interconnects</strong></td>
<td>Easy</td>
<td>Not available</td>
</tr>
<tr>
<td><strong>Horizontal interconnects</strong></td>
<td>Difficult</td>
<td>Easy</td>
</tr>
<tr>
<td><strong>Control of fabrication process</strong></td>
<td>Easy</td>
<td>Difficult</td>
</tr>
<tr>
<td><strong>Fabrication cost</strong></td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Sensitivity of electrical properties to fabrication process</strong></td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

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Hybrid CNT+graphene interconnecting structure..

D. Kondo, S. Sato, and Y. Awano,

Self-Organization of Novel Carbon Composite Structure: Graphene Multilayers Combined Perpendicularly with Aligned Carbon Nanotubes

Applied Physics Express, 2008

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Real-world examples of successful CMOS-CNT integration.

Pillars made by CNTs bundle
CNT pillar bumps for flip-chip high power amplifier

Soga et al. Proc. ECTC, 2008
Real-world examples of successful CMOS-CNT integration.

Carbon nanotubes as on-chip interconnects:
A 1GHz IC with CNT bundle interconnects wiring CMOS

Close et al. Nano Letters 2008

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Real-world examples of successful CMOS-CNT integration.

Carbon nanotubes and graphene on-chip interconnects:
CMOS ring oscillator

Carbon interconnect modeling: final goal for IC designers

**ELECTROMAGNETIC MODEL**

- Maxwell equations

**Carbon interc, electrodynamical model**

- heuristic approaches (e.g., Luttinger liquid theory)
- quasi-classical approaches (e.g., Boltzmann equation, fluid models,..)

**CIRCUIT MODEL**

The final goal is a **simple** but **physically meaningful** circuit description of the “channel”:

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Non-local Ohm law for a generic CNT shell

\[
\left( \frac{i \omega}{v} + 1 \right) J_z = \frac{1}{v \left( \frac{v}{i \omega} + 1 \right)} v_F^2 \frac{\partial \rho_s}{\partial z} + \sigma_c E_z
\]

Validity limits:
- Low bias conditions \( E_z < 0.54 \, V / \mu m \)
- Low frequency \( f < 1 \, THz \)


Transmission line model for an isolated CNT shell or GNR sheet

PUL parameters

\[
L' = \frac{L'_m + L'_k}{\alpha_c}
\]

\[
C' = C'_e
\]

\[
R' = \frac{v_F L'_k}{l_{mfp} \alpha_c}
\]

\[
L_k = \frac{R_0}{2v_F M}
\] Kinetic inductance

\[
a_C = 1 + \frac{C'_e}{C'_Q}
\]

\[
C'_Q = \frac{2M}{v_F R_0}
\] Quantum capacitance

MODEL PARAMETERS:

- Number of conducting channels \( M \)
- Mean free path \( l_{mfp} \)

\( R_0 = 12.9k\Omega \)

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Transmission line model for CNTs

Typical conditions

\[ C_e' \ll C_Q', \quad L_m' \ll L_k' \]

\[ a_C \approx 1, \quad L' \approx L_k' \]

\[ R' \approx \nu L_k' = \frac{\nu F}{l_{mfp}} L_k' \]

The inductance is dominated by the kinetic term

NO – low propagation velocity

OK – insensitivity to high-frequency effects (skin and proximity effect)

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Impact of the resistance

Resistance model for a single CNT shell or a single GNR

\[ R_{\text{tot}} = \frac{R_0 + R_{\text{con}}}{M} + R'l \]

\[ R_{\min} = \frac{R_0}{M} = 6.45k\Omega \quad (\text{for } M = 2) \]

Bundles of CNTs or arrays of GNRs fed in parallel must be used!!
Circuit model identification: fittings for model parameters

**Number of conducting channels:**

\[
M \approx \begin{cases} 
0 & \text{for semicond. SWCNTs} \\
2 & \text{for metallic SWCNTs} \\
\frac{a_1 DT + a_2}{\alpha - \beta T} & \text{for MWCNTs} \\
\frac{M_0(W)}{\beta - \alpha} & \text{for GNRs}
\end{cases}
\]

*rigorously computed in:*


**Mean free path:**

\[
\frac{1}{l_{mfp}} = \frac{k_1 + k_2 T + k_3 T^2}{D}
\]

**CNT**

\[
\frac{1}{l_{mfp}} = \frac{\gamma}{W}
\]

**GNR**

*The fitting coefficients depend on the temperature and size ranges*


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Model validation - CNT

Static parameters (resistance)

Dynamic parameters (S-param.)

<table>
<thead>
<tr>
<th></th>
<th>our model</th>
<th>measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>S_{11}</td>
<td>$</td>
</tr>
<tr>
<td>$</td>
<td>S_{21}</td>
<td>$</td>
</tr>
</tbody>
</table>


J.J. Plombon et al., APL, 2007

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Model validation - GNR

A. Naeem and J. D. Meindl, 

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Signal integrity performance of on-chip CNT interconnects

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<table>
<thead>
<tr>
<th>22 nm node</th>
<th>global</th>
<th>interm.</th>
<th>local</th>
</tr>
</thead>
<tbody>
<tr>
<td>W [nm]</td>
<td>160.00</td>
<td>44.00</td>
<td>22.00</td>
</tr>
<tr>
<td>H [nm]</td>
<td>96.00</td>
<td>44.00</td>
<td>44.00</td>
</tr>
<tr>
<td>Rdr [kΩ]</td>
<td>0.16</td>
<td>0.81</td>
<td>8.09</td>
</tr>
<tr>
<td>Cout [fF]</td>
<td>4.90</td>
<td>0.98</td>
<td>0.09</td>
</tr>
<tr>
<td>CL [fF]</td>
<td>14.00</td>
<td>2.80</td>
<td>0.28</td>
</tr>
</tbody>
</table>
Local level

- SWCNT
  - DR=3 GB/s, rs 33 ps
  - DR=5 GB/s, rs 20 ps
  - DR=10 GB/s, rs 10 ps

- Cu

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Intermediate level

**MWCNT**

**Cu**

DR=1 GB/s

DR=10 GB/s

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Hybrid CNT /GNR/Cu on-chip interconnect

Temperature distribution

Metal 1 temperature = 378K

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Performance at 1GB/s (400K)

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Performance at 5 GB/s (400K)

Cu  CNT+Cu  CNT+GNR(1)  CNT+GNR(2)
Performance at 10 GB/s (400K)

Cu  CNT+Cu  CNT+GNR(1)  CNT+GNR(2)

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### Summary: electrical performance vs copper interconnects

<table>
<thead>
<tr>
<th></th>
<th>Local interconnects</th>
<th>Global interconnects</th>
<th>On-chip Vias</th>
<th>Chip-to-package interconnects</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SWCNT</strong></td>
<td>Comparable or better (depending on the metallic fraction)</td>
<td>Comparable or better (depending on the metallic fraction)</td>
<td>Comparable or better (depending on the metallic fraction)</td>
<td>Comparable or better (depending on the metallic fraction)</td>
</tr>
<tr>
<td><strong>MWCNT</strong></td>
<td>comparable</td>
<td>better</td>
<td>worse</td>
<td>better</td>
</tr>
<tr>
<td><strong>GNR</strong></td>
<td>comparable</td>
<td>worse or better (strongly depending on the edge effect and doping)</td>
<td>Not available</td>
<td>Not available</td>
</tr>
</tbody>
</table>

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Conclusions

• **Carbon-based interconnects** are proposed to replace copper for on-chip interconnects for technology nodes of 22 nm and below.

• **Carbon nanotubes** and **graphene nanoribbons** are candidate to realize them. First examples of monolithic CNT/CMOS and GNR/CMOS integration.

• **Circuit models** for carbon interconnects may be derived in the frame of the TL theory. Besides classical parameters, quantistic terms appear (such as kinetic inductance and quantum capacitance) which strongly affect the electrical behavior.

• **A simple model has been proposed and validated**, based on fittings of the physical parameters. The fitting formulas are function of temperature and size.

• Signal integrity analysis show the potential electrical performance of the proposed solutions, some of them strongly influenced by the possibility to have good control in fabrication process.
Thank you