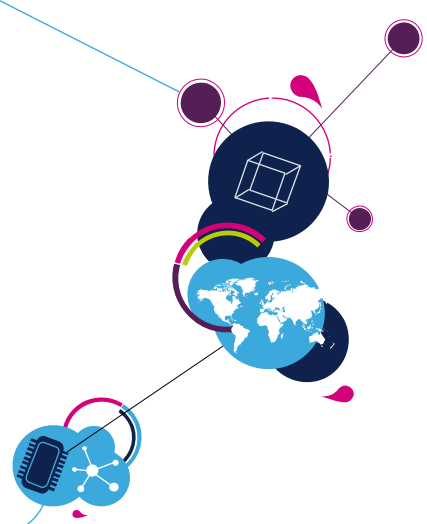
SSO Noise And Conducted EMI: Modeling, Analysis, And Design Solutions



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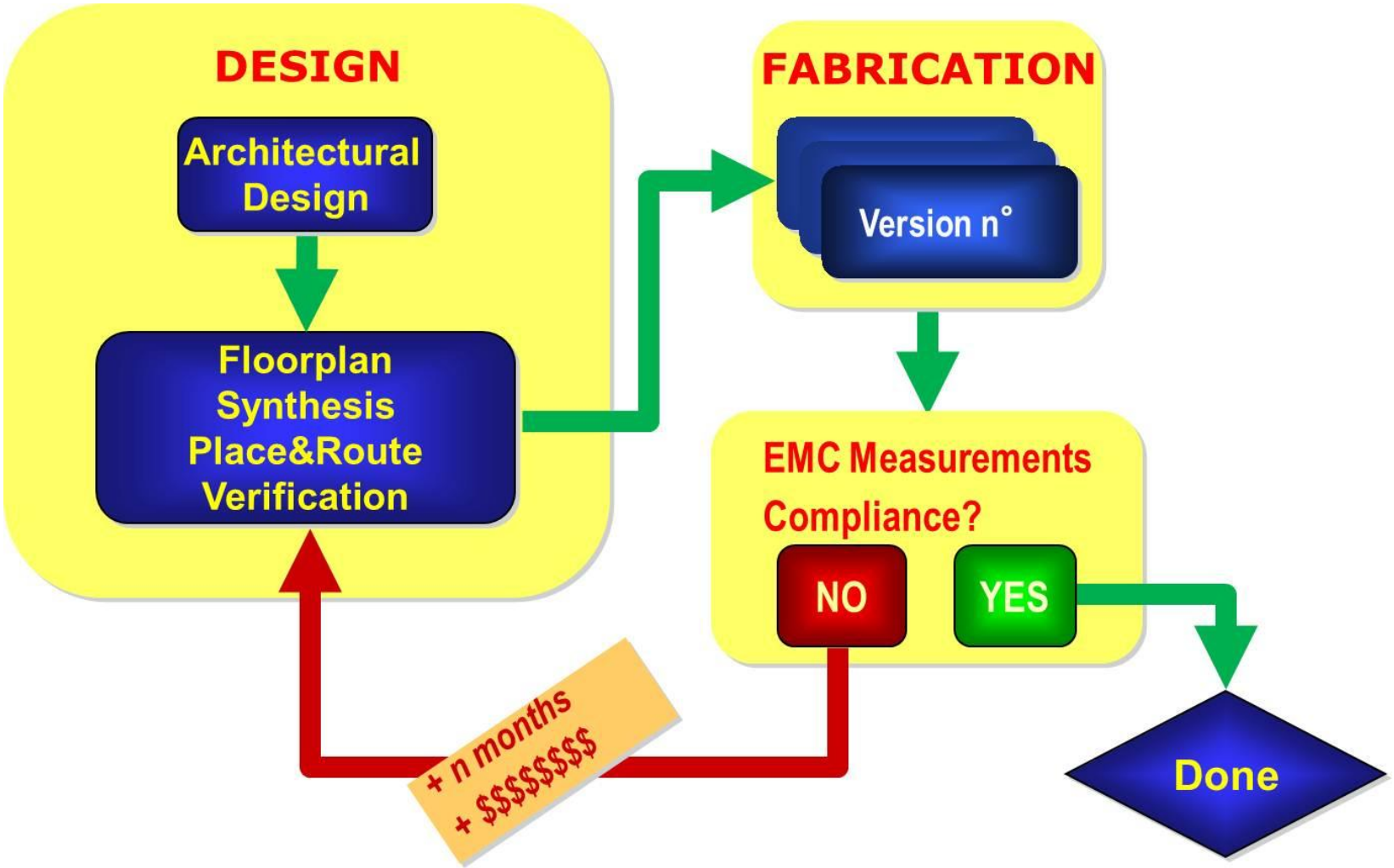
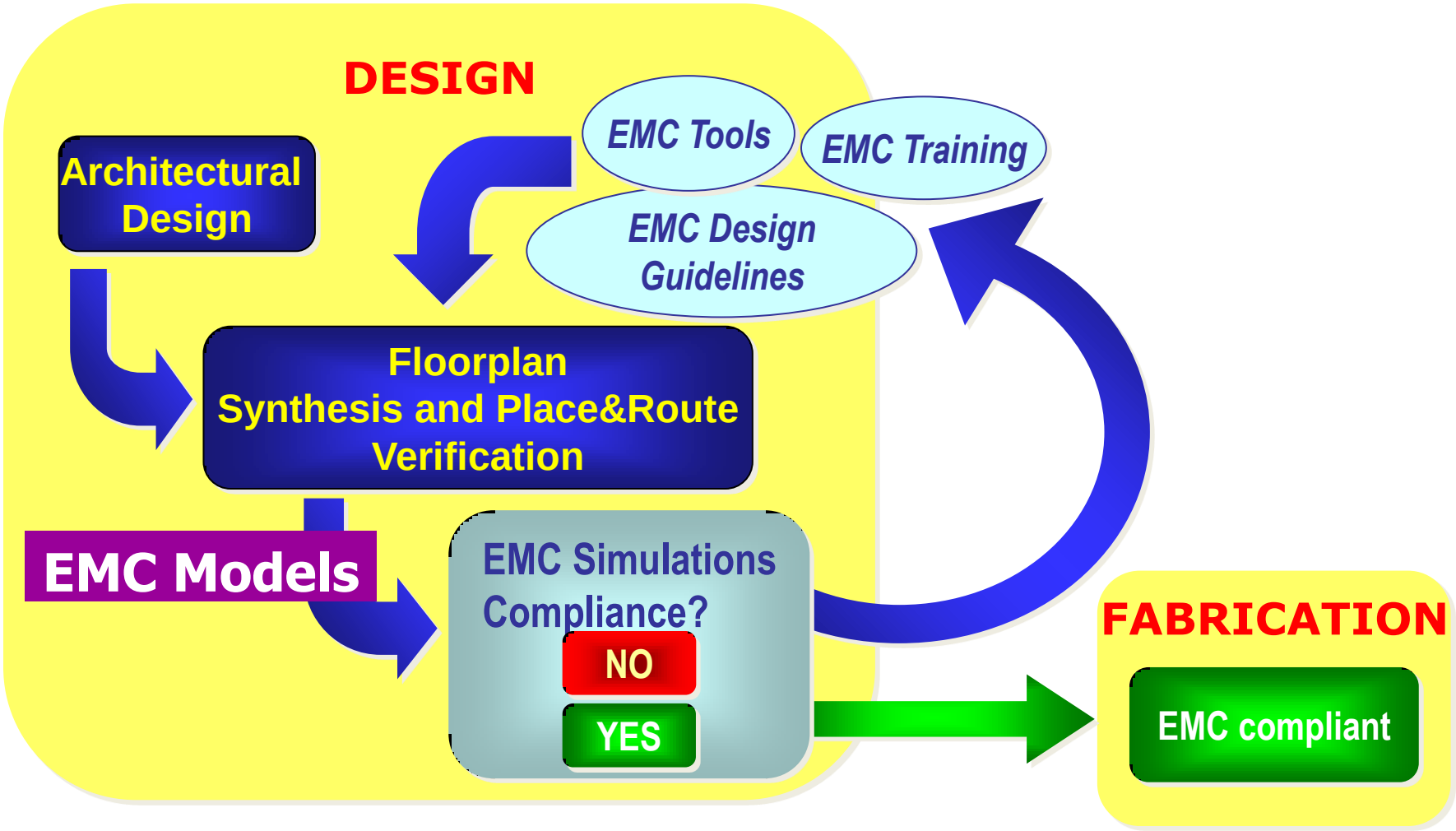
Today's I/Os Challenges

- Higher I/O count
- Increasing operating frequencies
- Faster signal edge rates
- High I/O density makes it difficult to place PCB decaps close enough to the pads
- Automotive specific challenge: I/Os signal conducted EMI
- EMC and signal integrity are another mandatory objective for first silicon success

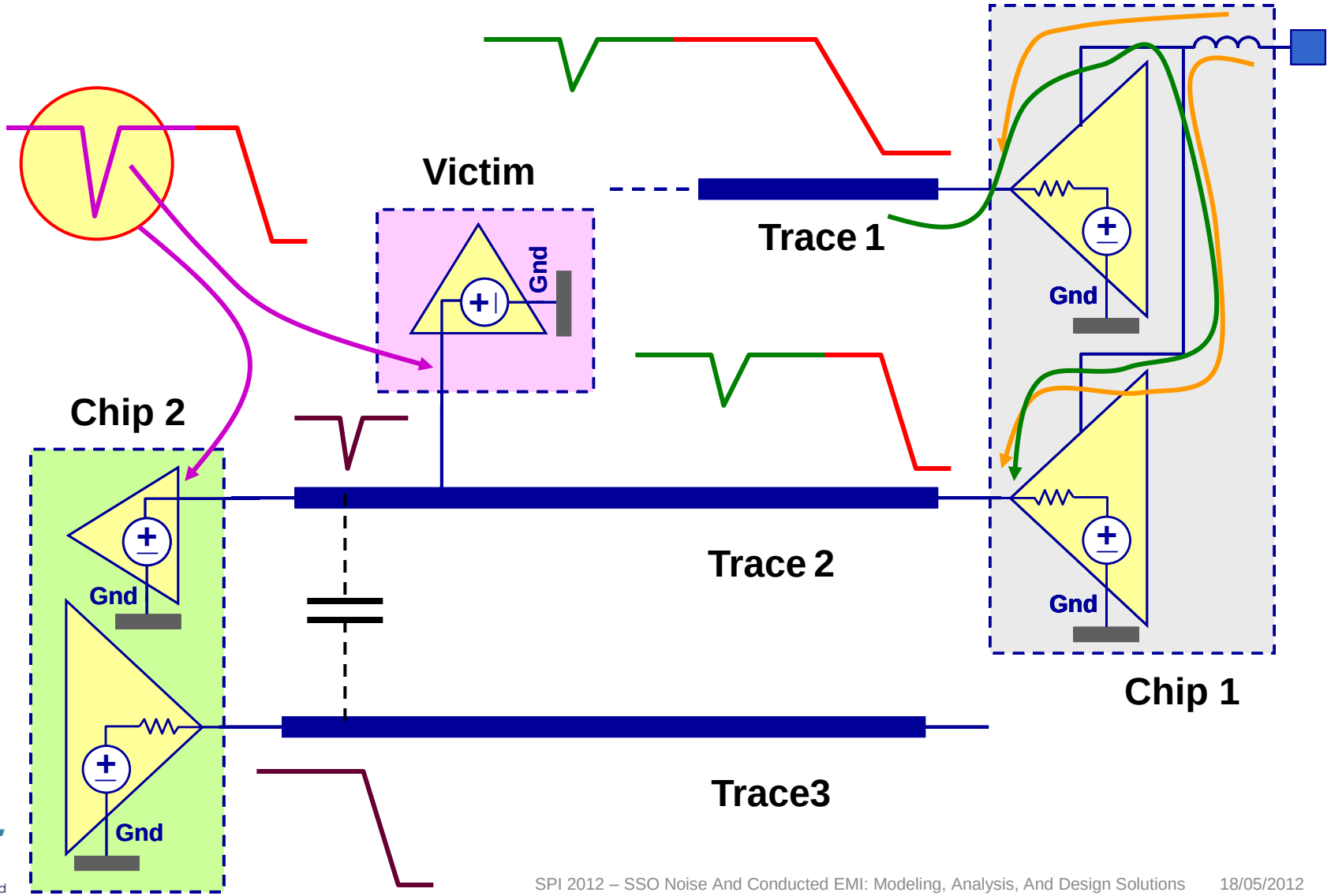
EMC At The End Of The Design Flow



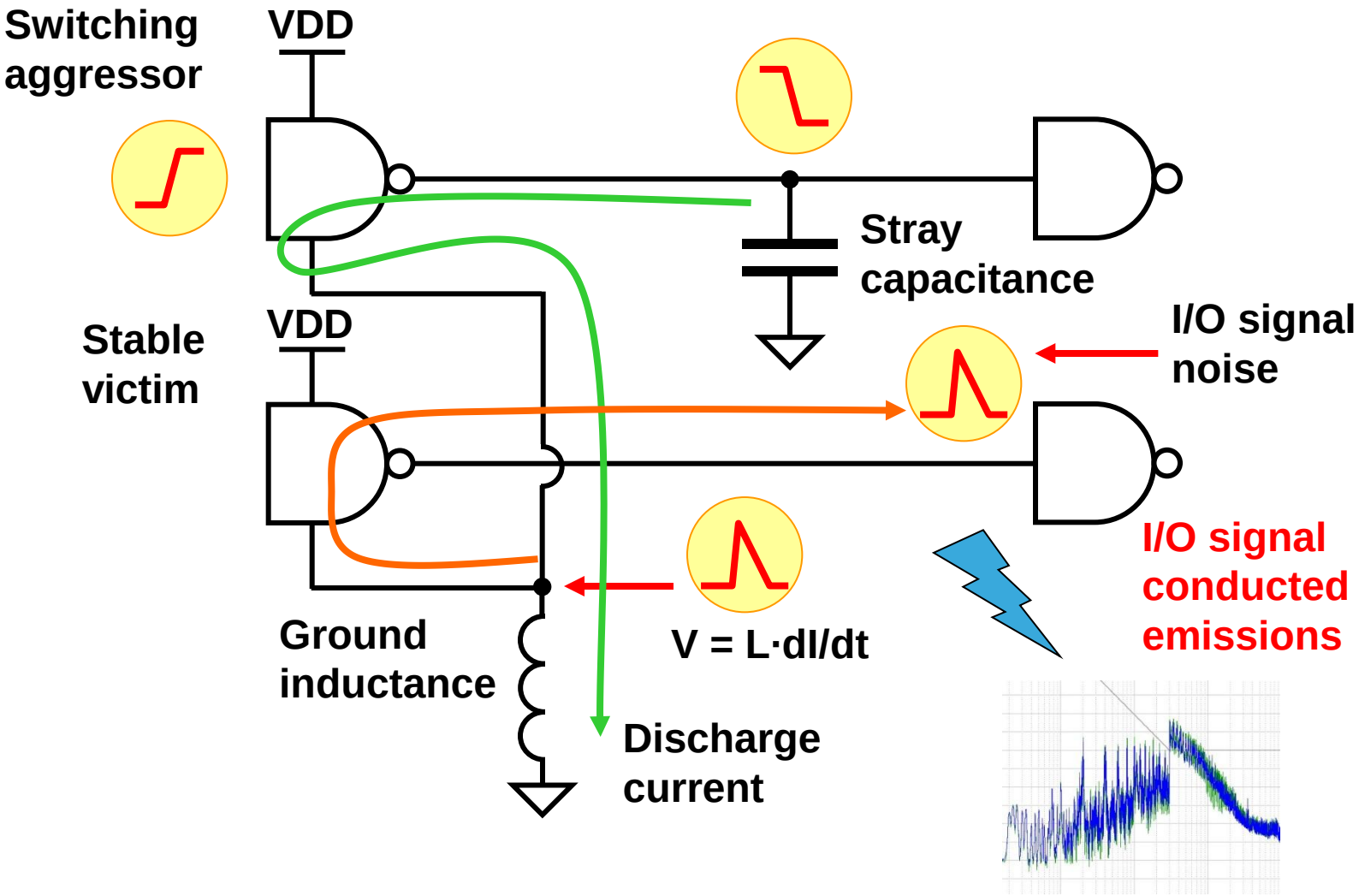
Our Vision: EMC-Aware Design



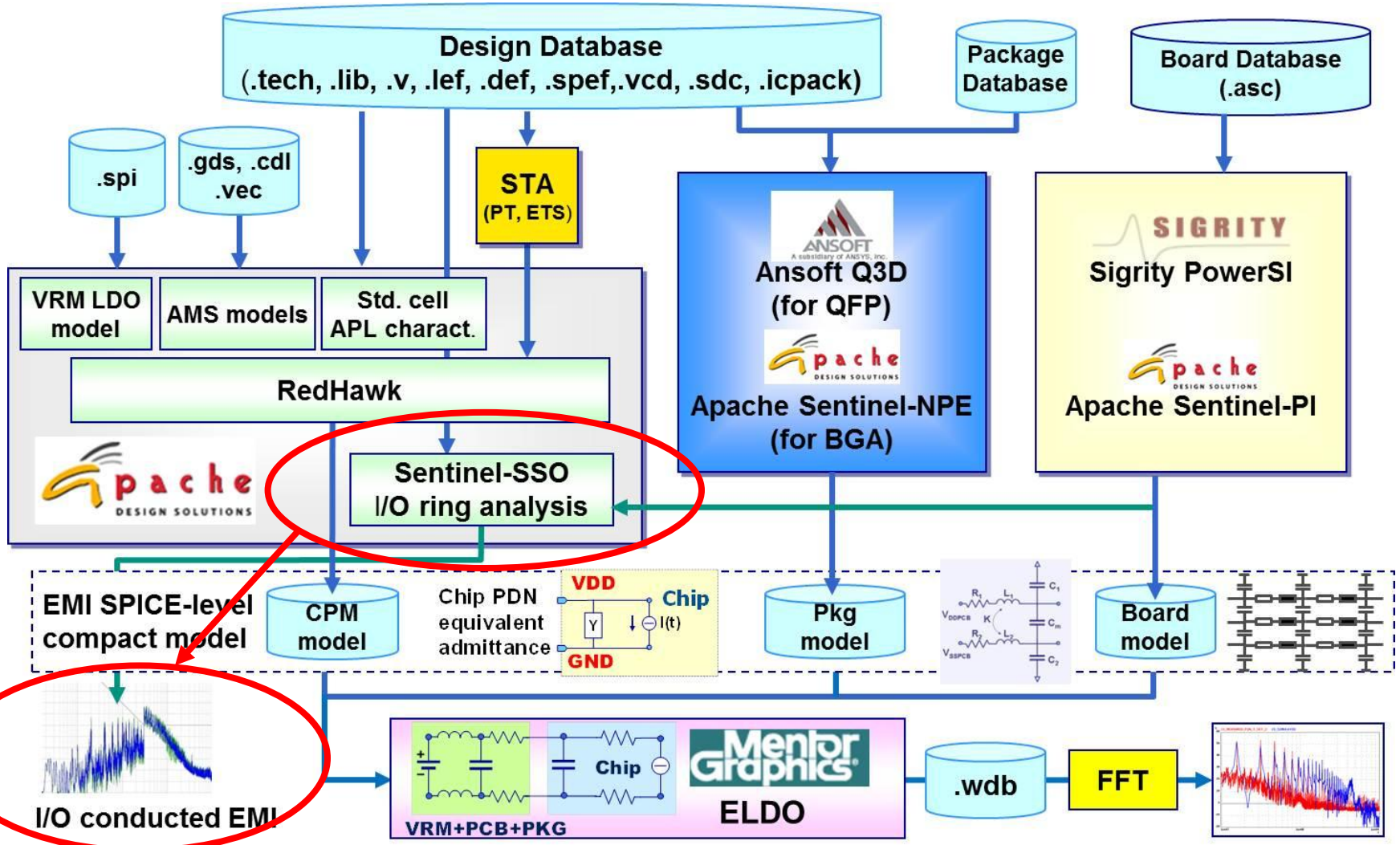
Reflection, Crosstalk, And SSO Noise



SSO Noise And Conducted EMI

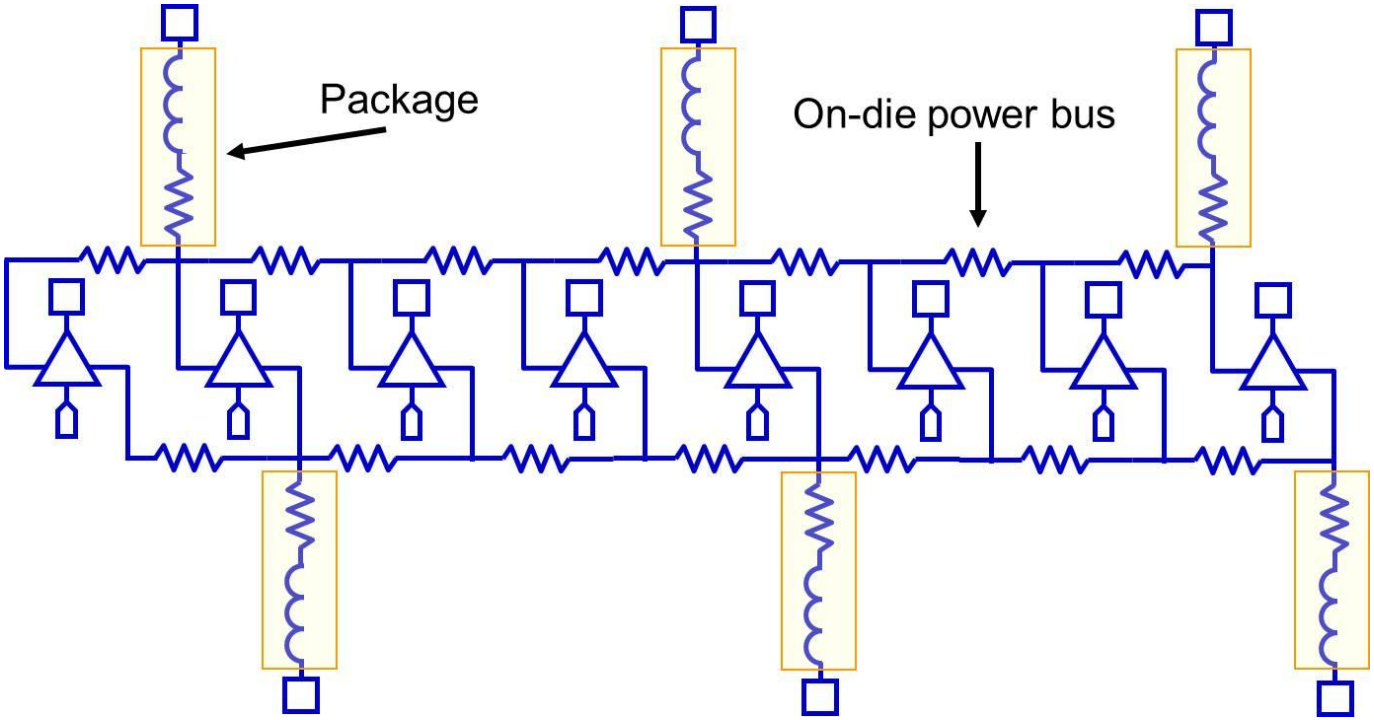


System-Level EMI Simulation Flow

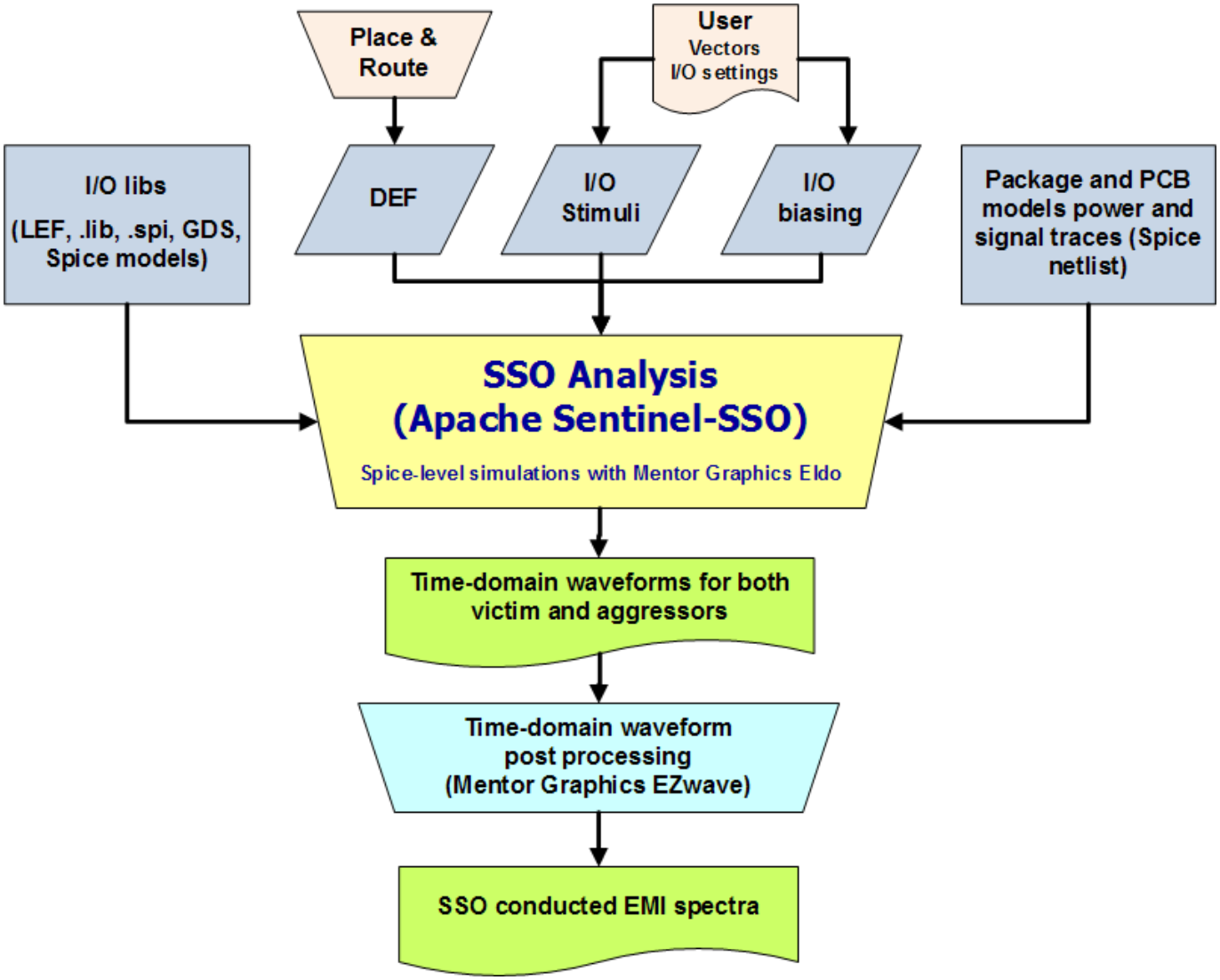


I/O Ring Circuit

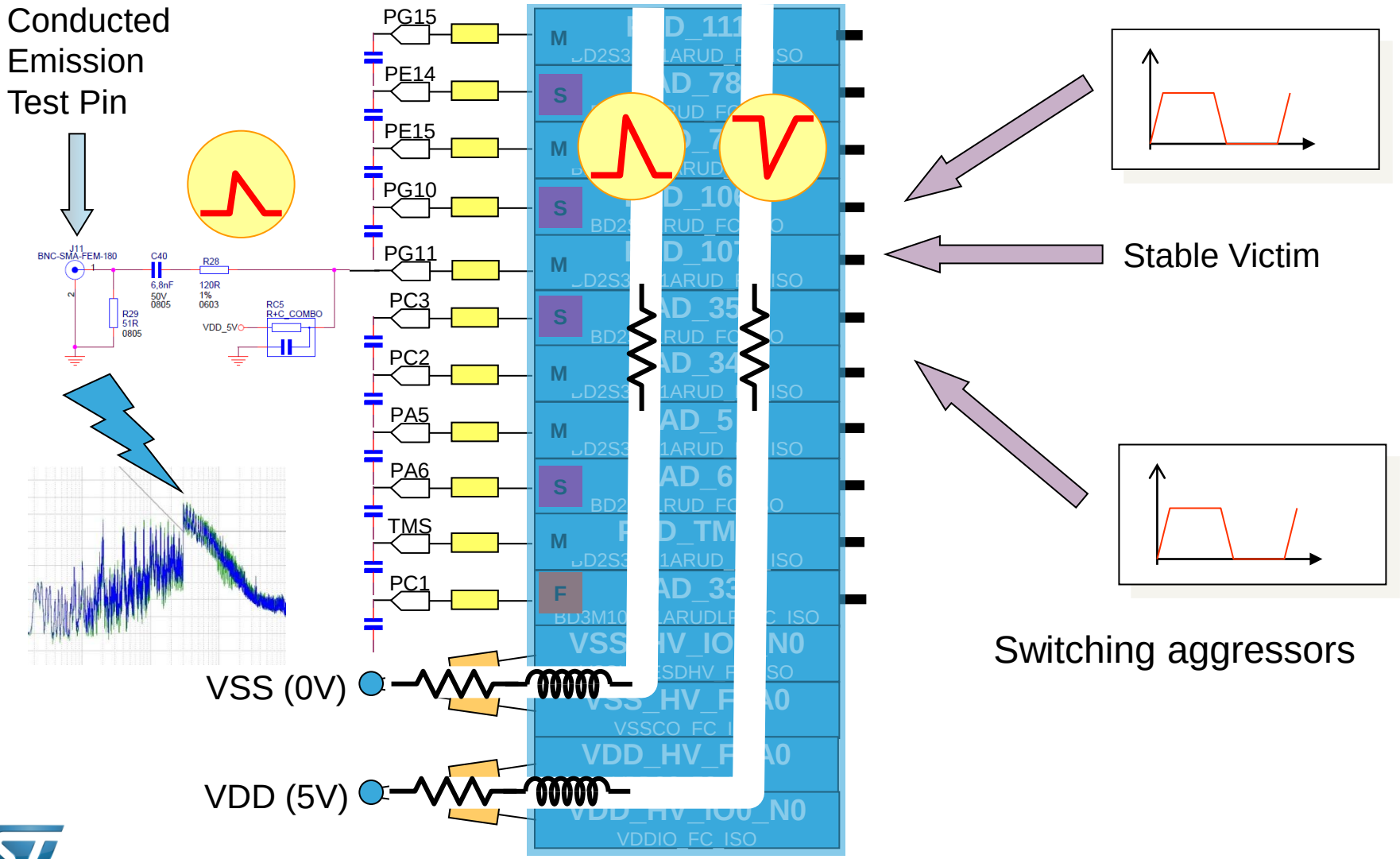
- Any realistic signal integrity and EMI simulation must include the complete system-level macromodel (die, package, board)
- A full transistor-level simulation of the I/O ring is impractical even for a limited number of adjacent toggling I/Os and a given victim



SSO Flow


Place & Route
User
Vectors
I/O settings
I/O libs
(LEF, .lib, .spi, GDS, Spice models)
DEF
I/O Stimuli
I/O biasing
Package and PCB models power and signal traces (Spice netlist)
SSO Analysis
(Apache Sentinel-SSO)
Spice-level simulations with Mentor Graphics Eldo
Time-domain waveforms for both victim and aggressors
Time-domain waveform post processing
(Mentor Graphics EZwave)
SSO conducted EMI spectra

I/O Bank For EMI Analysis



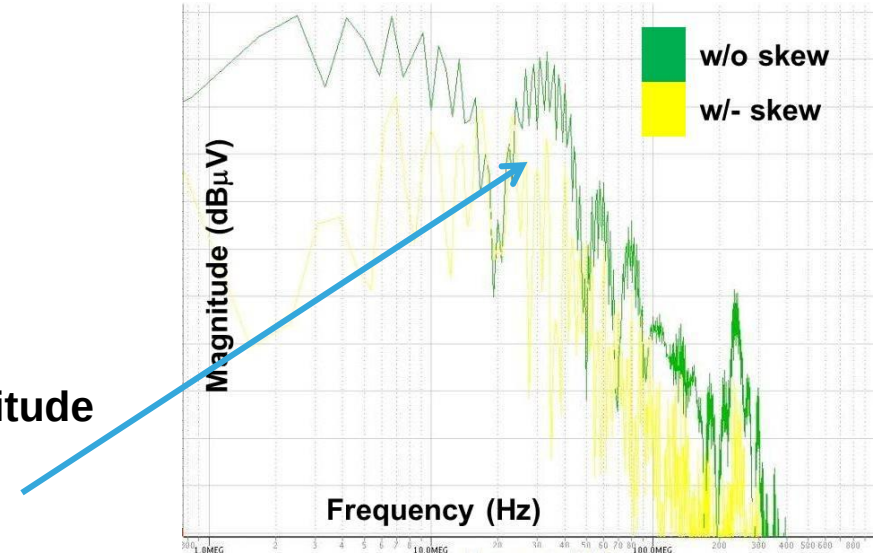
Design Solutions For SSO Noise Reduction

- I/Os' signal skewing
- I/O ring fillercap insertion
- I/O pads reduced driving strength
- I/O ring power/ground supply placement

I/O Skewing Impact on EMI

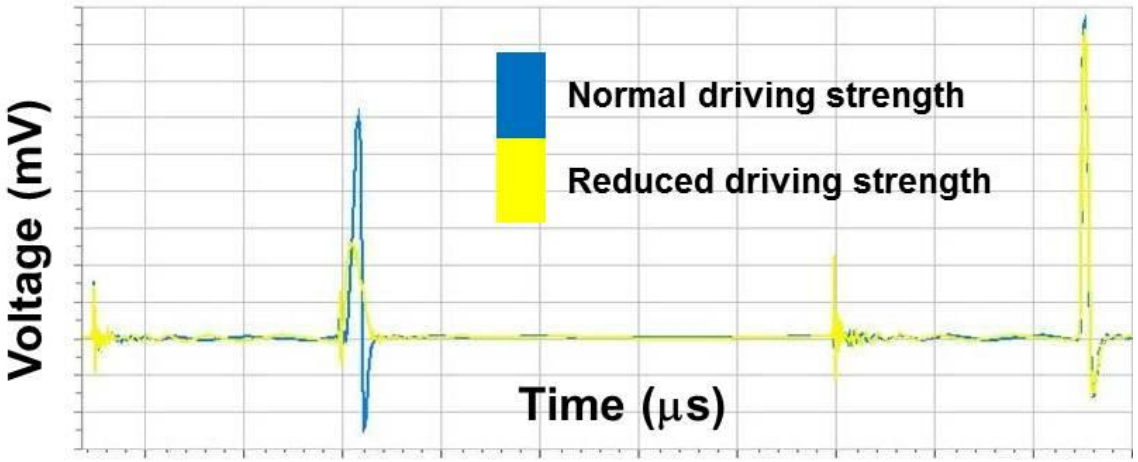
- Typical I/Os' working frequency for automotive applications are in the range of a few KHz and do not need to toggle synchronously
  - A relative skew in the range of about 10ns is compatible with a correct functionality of the I/O ring
- Harmonic amplitude reduction of several dBµVs obtained in the frequency range of 1GHz

On some critical harmonics amplitude reduction of about 10dBµV



I/O Fillercaps Insertion And Driving Strength Reduction

- I/O fillercap insertion did not prove to be an effective technique
  - Huge amount of decaps and related area to achieve only few dBµV amplitude reduction
  - Difficult to exploit this technique on typical pad-limited I/O rings
- I/O driving strength reduction (when compliant with the timing constraints) from MEDIUM to SLOW strength version can further reduce the SSO noise

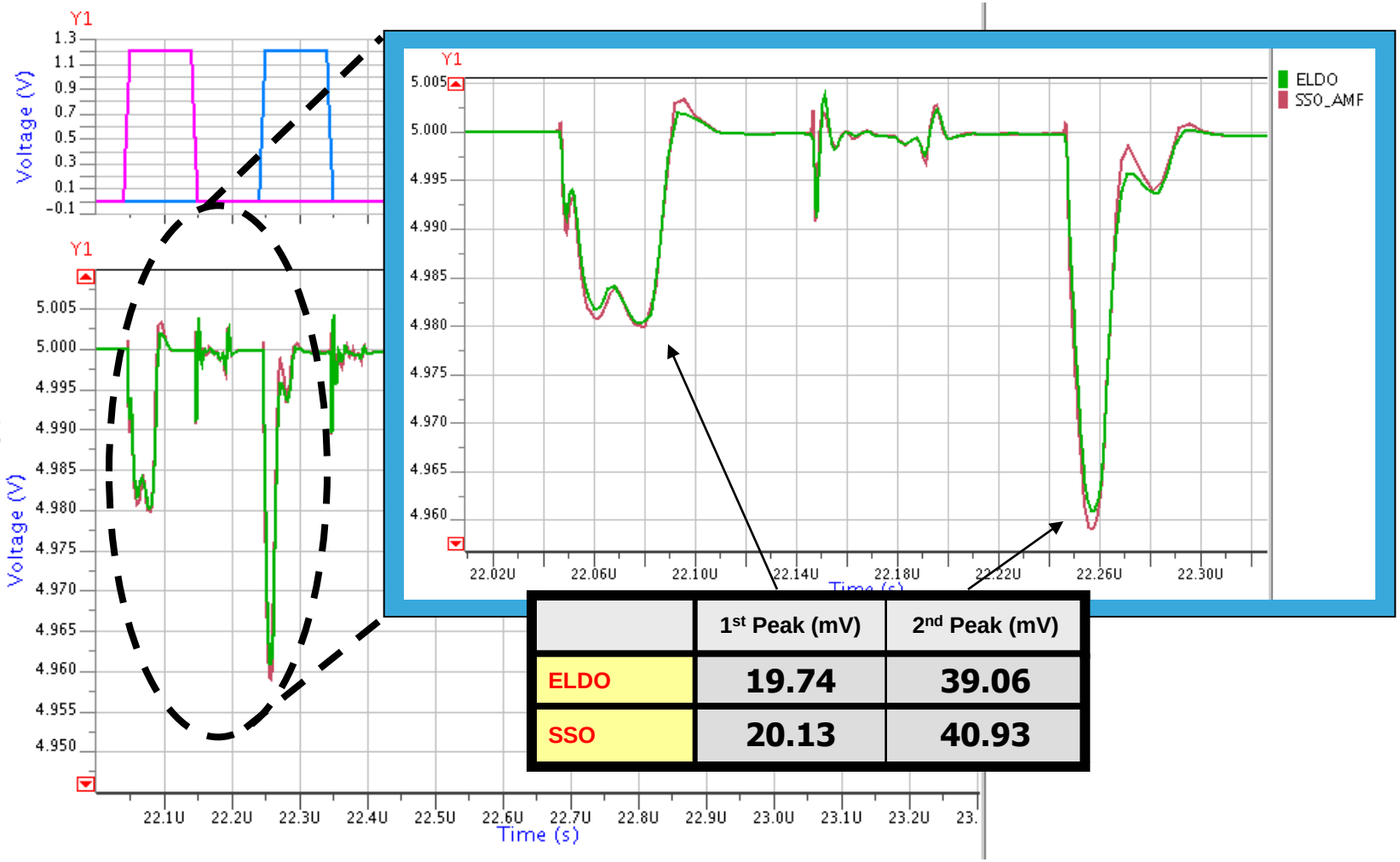


SSO Flow Validation

- The gate-level SSO flow was validated vs. full Spice-level simulations

Aggr. PADs Input

Victim PAD Output



	1st Peak (mV)	2nd Peak (mV)
ELDO	19.74	39.06
SSO	20.13	40.93

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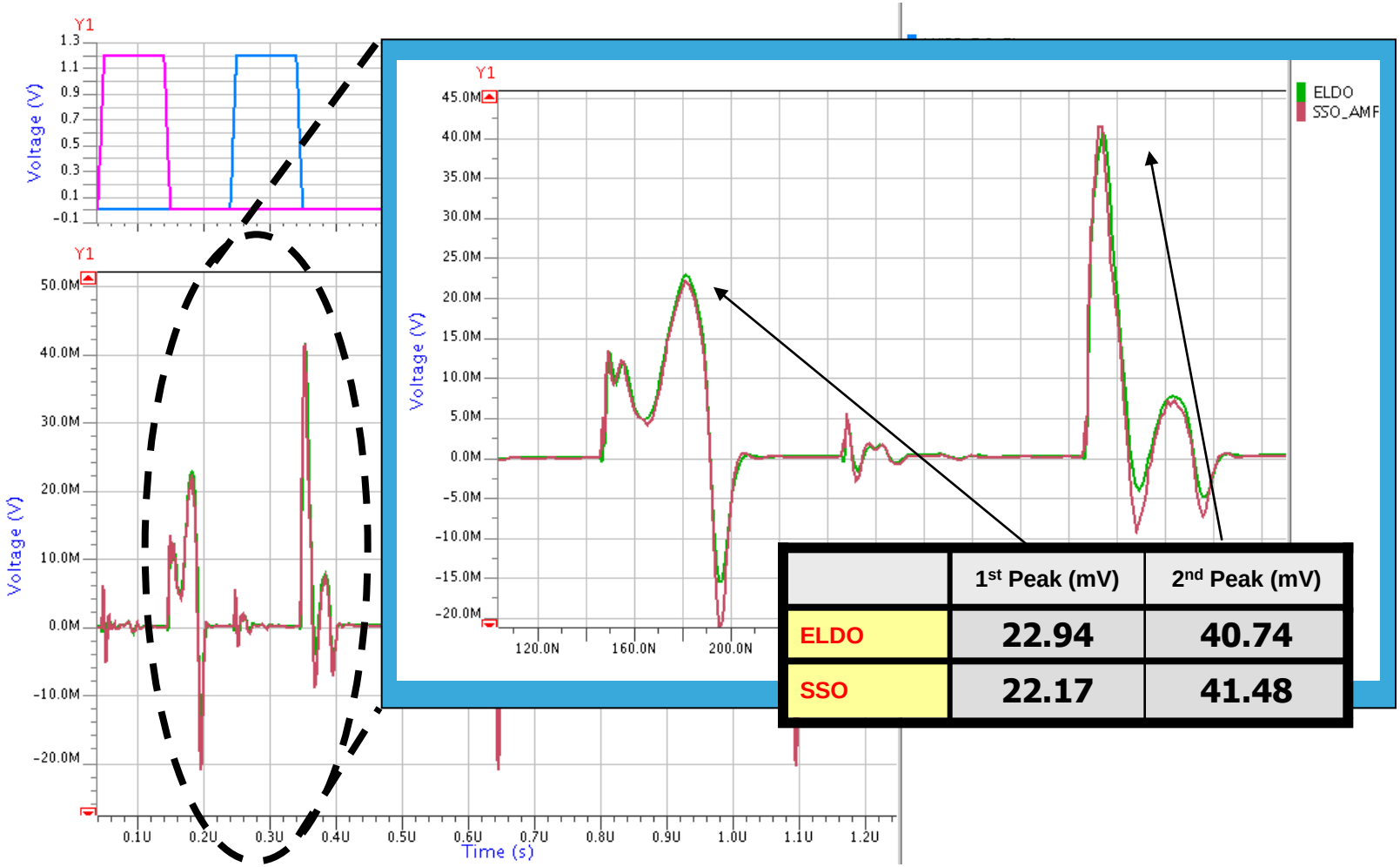
Aggr. PADs Input

Victim PAD Output



	1st Peak (mV)	2nd Peak (mV)
ELDO	22.94	40.74
SSO	22.17	41.48

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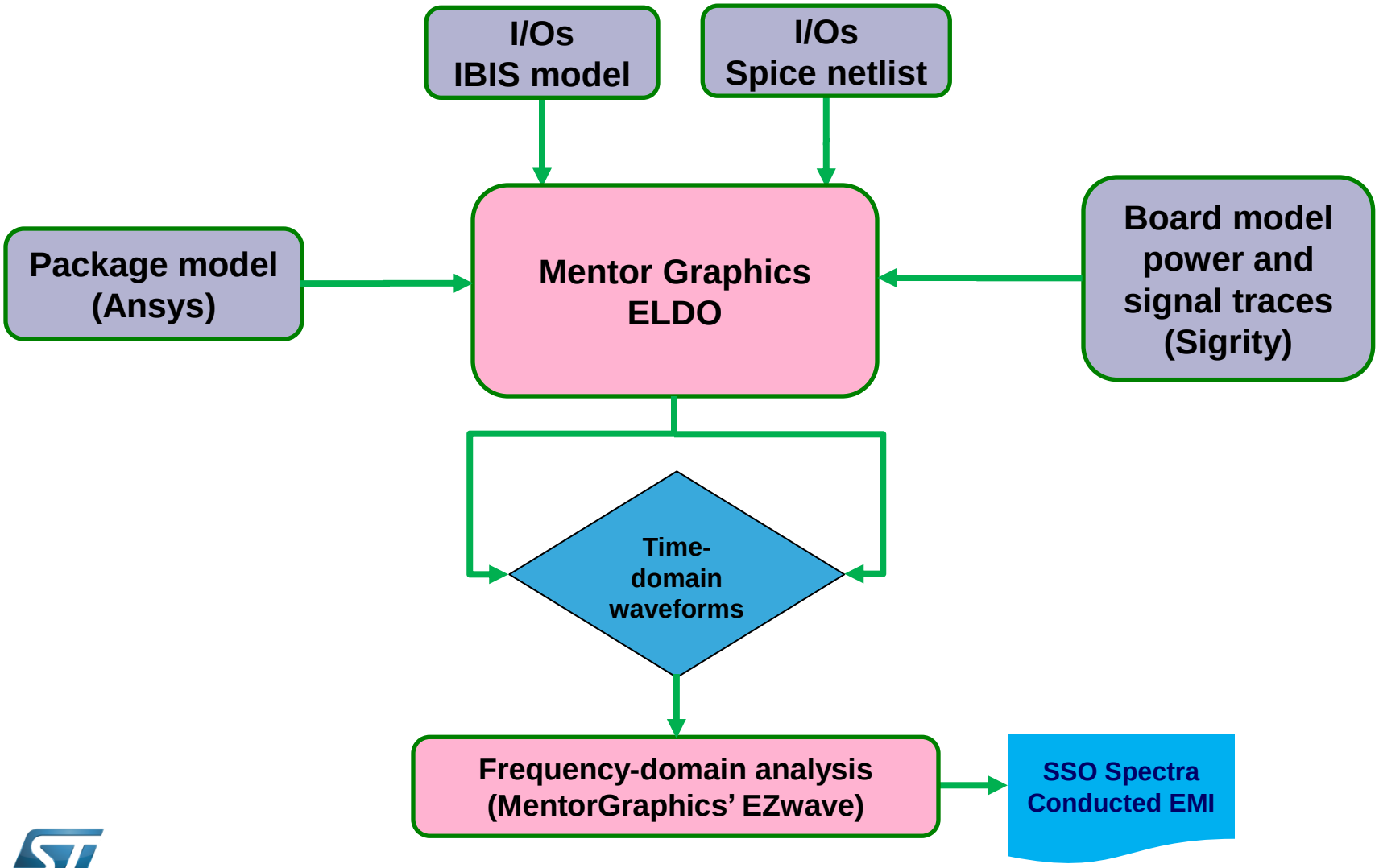
IBIS For SSO And EMI Analysis

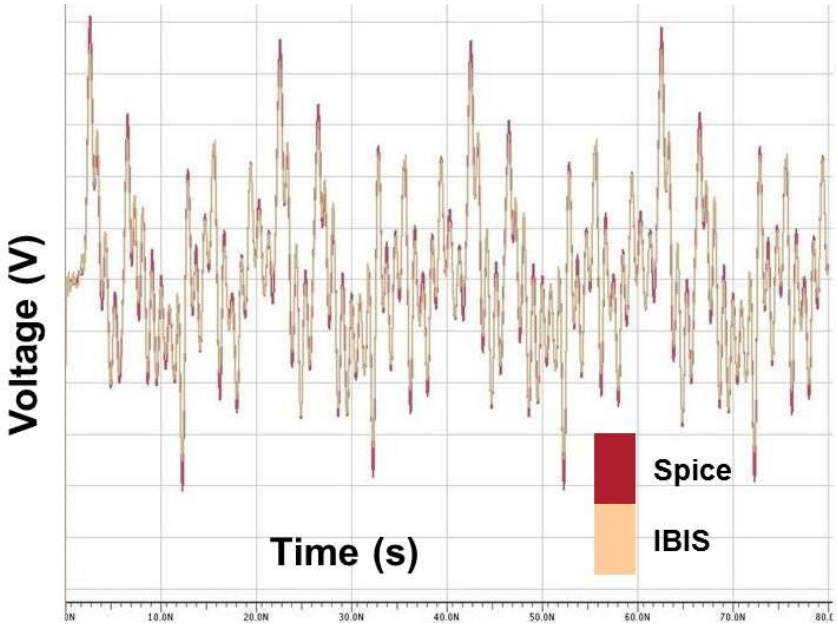
- Traditionally IBIS models have been used for signal integrity simulations on system PCBs
  - Behavioral modeling
  - IP protection
  - Fast simulation time
  - Reasonable accuracy
- However IBIS v4.0 cannot include predriver and crossbar currents and I/O ring power/ground supply bouncing which is the dominant source of SSO and conducted EMI
- To validate IBIS v5.0 for EMI analysis the same STYY I/O bank was used
- IBIS v5.0 was compared vs. full transistor-level simulations

IBIS Validation Flow

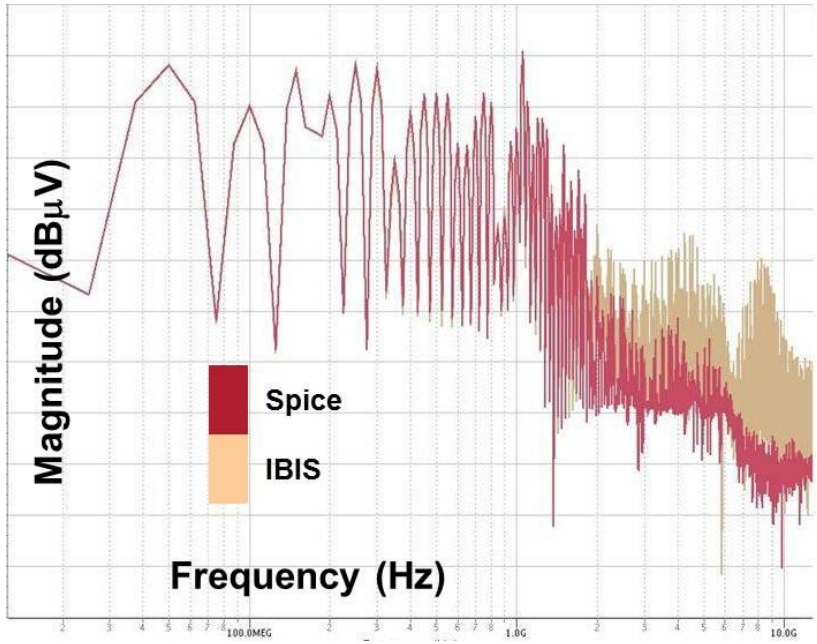


IBIS For SSO And EMI Analysis

IBIS v5.0 vs. Spice



Time-domain analysis



Frequency-domain analysis

IBIS vs. Spice: good accuracy up to 2GHz

Summary

- CAD flow and design solutions for SSO and I/O conducted EMI analysis and optimization were presented
- Methodology exploited on an industrial automotive microcontroller in ST 90nm with eNVM technology
- IBIS v5.0 can be used for a reliable SSO and EMI analysis