Skinny Trace Compensation Methodology for High Speed Serial Interface

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Agenda

• Skinny Trace Compensation
  – Description
  – Computation
  – Implementation
  – HDMI Channel
  – PCB Layout and Extraction
  – Improvements
  – Conclusion
Skinny Trace Compensation Technique

\[ Z_0 = \sqrt{\frac{(x \cdot v) (kZ_0)}{(x \cdot v) + C_L kZ_0}} \]

\( Z_0 \): Characteristic impedance of regular transmission line

\( v \): Unloaded trace propagation constant

\( k = Z_L/Z_0 \): Ratio of impedance for the skinny and the regular segments

\( C_L \): Capacitance of the load

Skinny Trace Implementation

Typical Layout transition

Improved Layout transition
HDMI Channel
Pre-layout Simulation Setup
Simulated Eye Diagram (pre-layout)
PCB Layout
Package and PCB Model Extraction

Package

PCB
Post-layout Circuit Simulation Setup

- Detailed spice netlist was used to represent the driver
- Pseudo-random bit sources with different seeds were used as inputs to the driver circuits
Simulated Eye diagram (post-layout)
Measurement
(Without Skinny Trace Compensation)
Measurement
(With Skinny Trace Compensation)
Model / Correlation: Before / After

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Conclusions

• Skinny Trace Compensation is an effective yet simple technique to address excess capacitive impedance in high speed channels.

• System level methodology for a high speed serial interface (HDMI) interface on a high-speed/low power mobile microprocessor SOIC design is presented.

• Excellent correlation between simulated and measured results were obtained.